

# Compal Confidential

## Schematics Document

Intel CLARKSFIELD/ARRANDALE  
with IBEX PEAK-M core logic

Cartier DIS

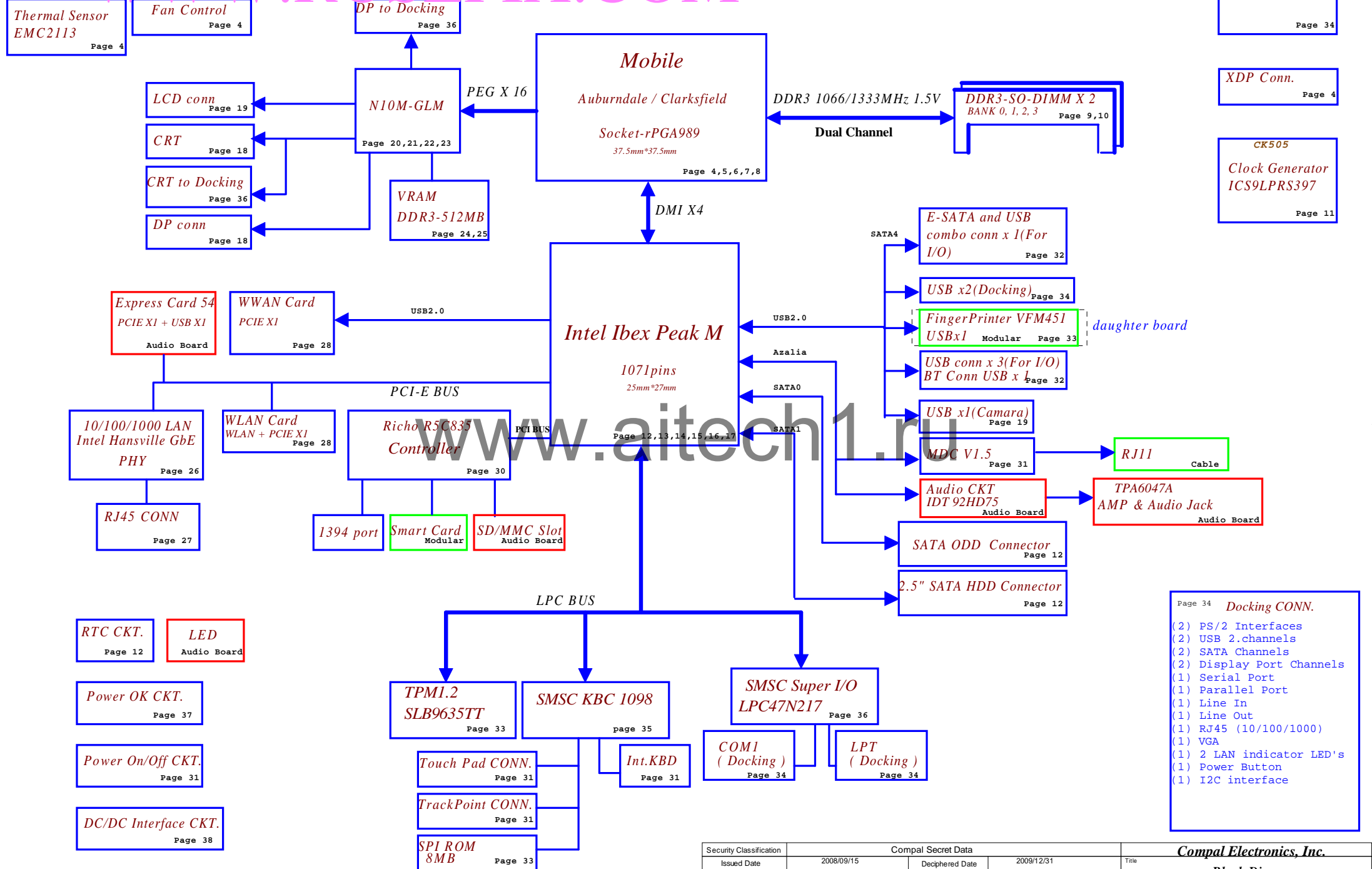
LA-4901P

2009-12-01

REV:1.0

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	產出人員	
	產出日期	
	解密日期	

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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title Cover Sheet		
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## Voltage Rails ( O MEANS ON X MEANS OFF )

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+3VM +1.05VM	+1.5V +0.75V	+5VS +3VS +1.5VS +VGA_CORE +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

### Symbol Note :



: means Digital Ground



: means Analog Ground

### Install below 45 level BOM structure

45@ : means just put it in the BOM of 45 level.

### Install below 43 level BOM structure

@ : means just reserve , no build

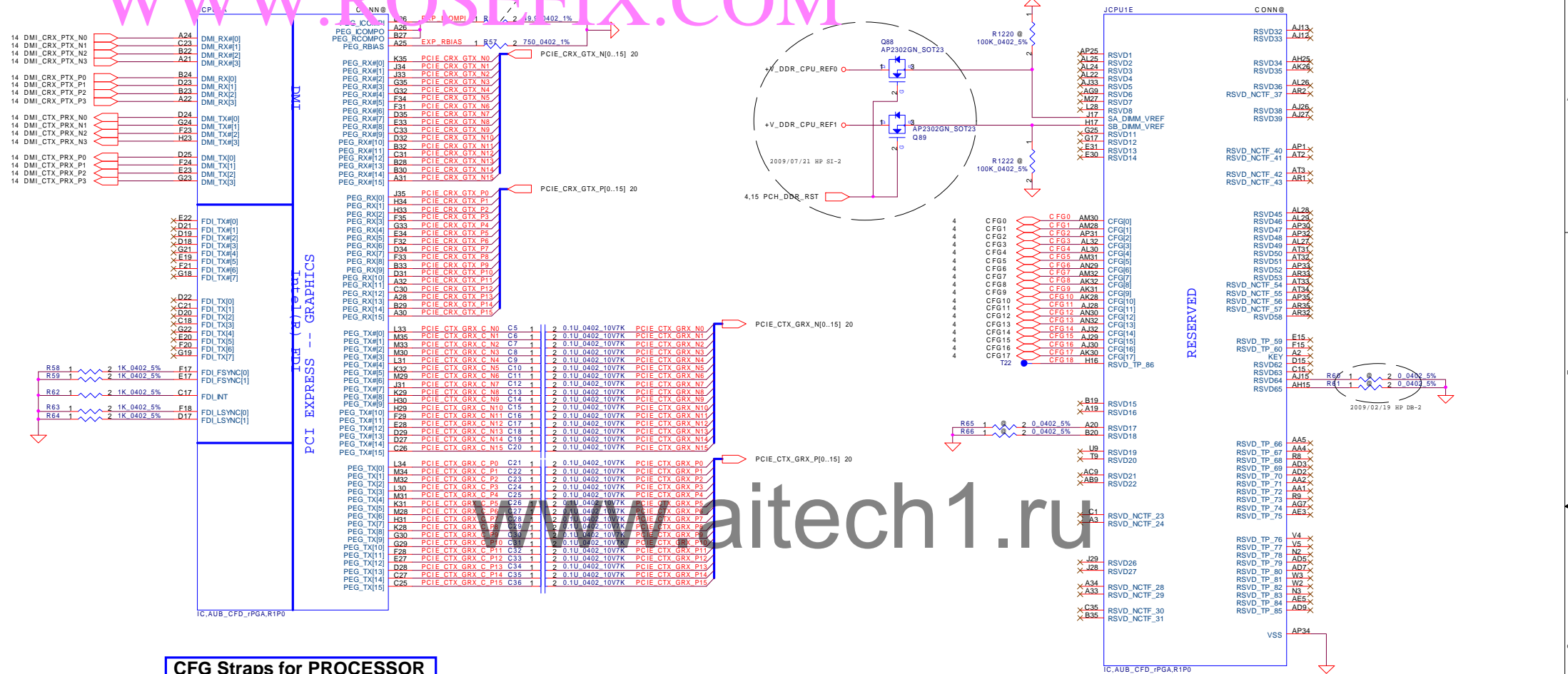
CONN@ : means ME part.

VRAM@ : means VRAM strip pin part.

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X





### CFG Straps for PROCESSOR

CFG0 R67 1 2 3.01K 0.402 1%

PCI-Express Configuration Select  
CFG0 1: Single PEG  
0: Bifurcation enabled  
Not applicable for Clarkfield Processor

CFG3 R69 1 2 3.01K 0.402 1%

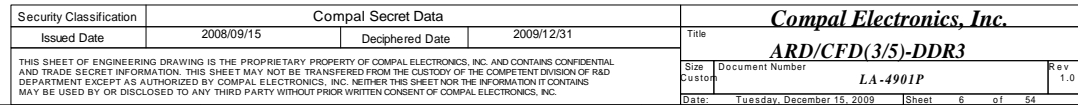
CFG3-PCI Express Static Lane Reversal  
CFG3 1: Normal Operation  
0: Lane Numbers Reversed  
15 -> 0, 14 -> 1, .....

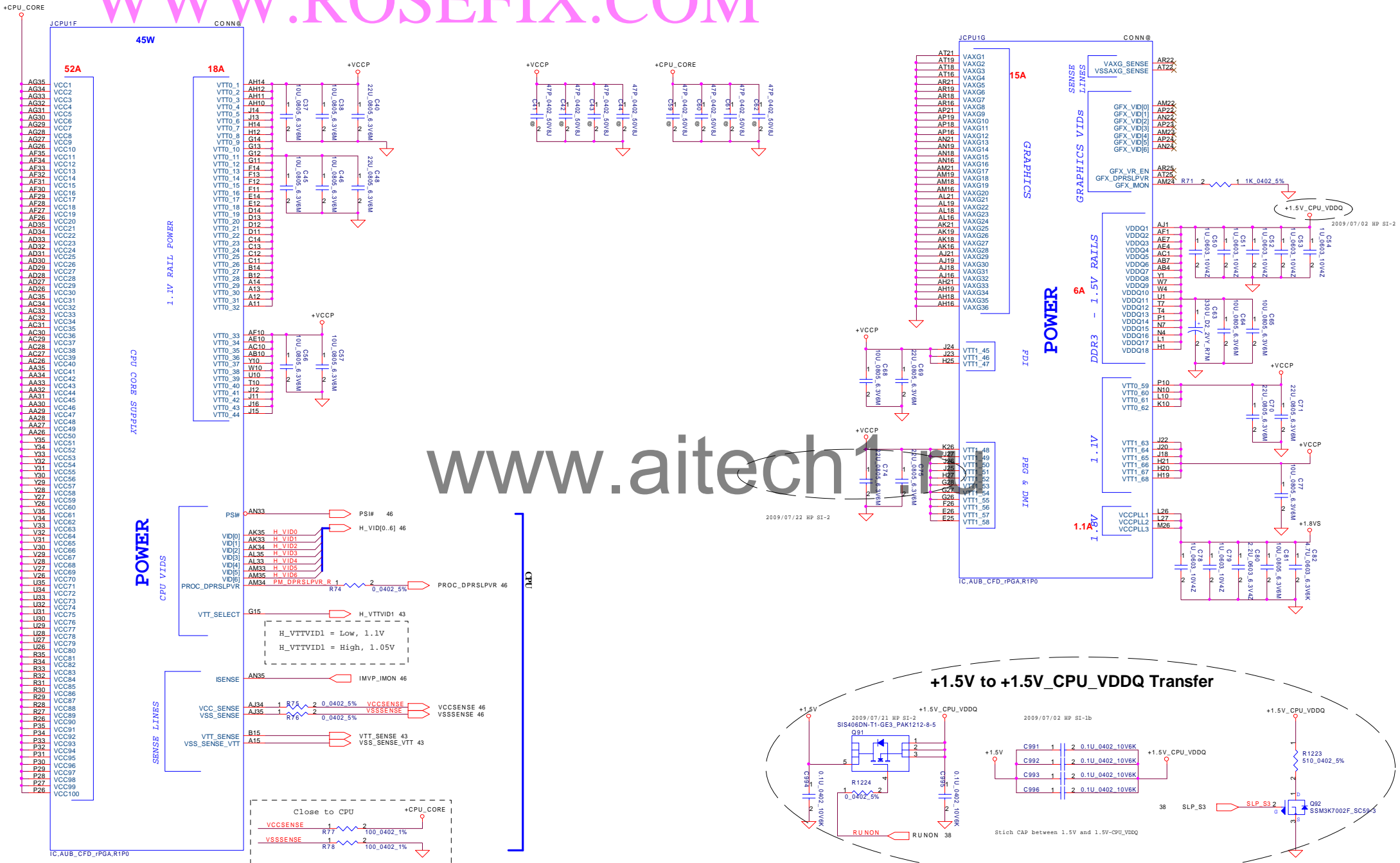
CFG4 R70 1 2 3.01K 0.402 1%

CFG4-Display Port Presence  
CFG4 1: Disabled: No Physical Display Port attached to Embedded Display Port  
0: Enabled: An external Display Port device is connected to the Embedded Display Port

CFG7 R68 1 2 3.01K 0.402 1%

Only temporary for early C/PD samples (rPGA/BGA)

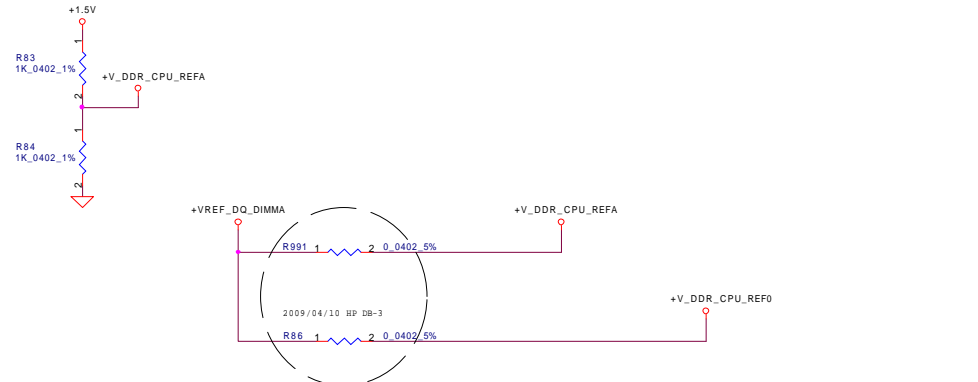
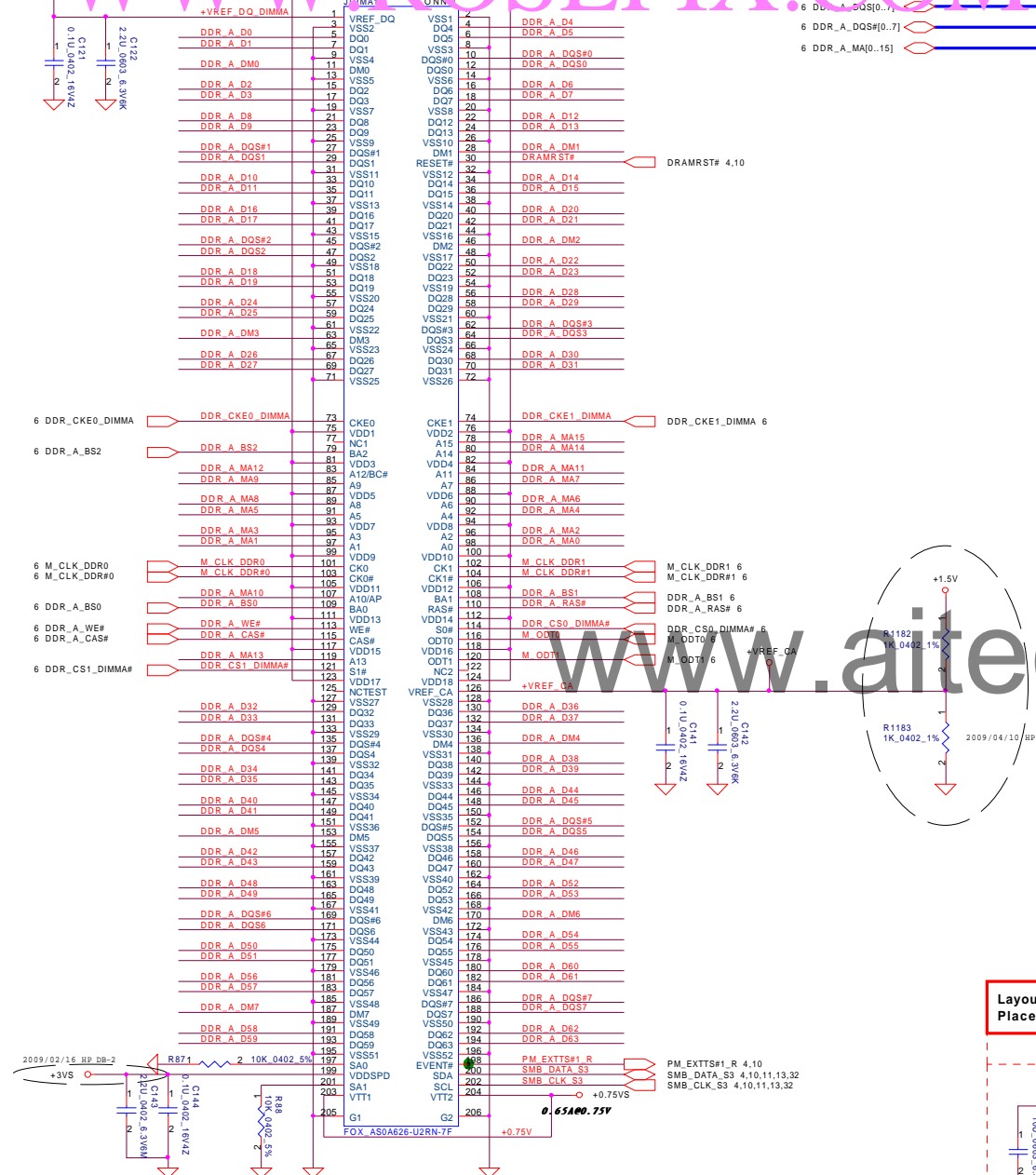









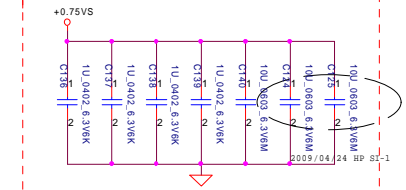
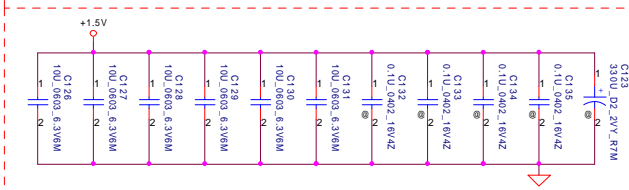
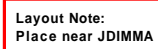
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\_RAS#  DDR\_A\_RAS# 6  
 CS0\_DIMMA#  DDR\_CS0\_DIMMA# 6  
 DT0  M\_DDT0 6  
 DT1  M\_DDT1 6  
 REF\_CA  +VREF\_CA

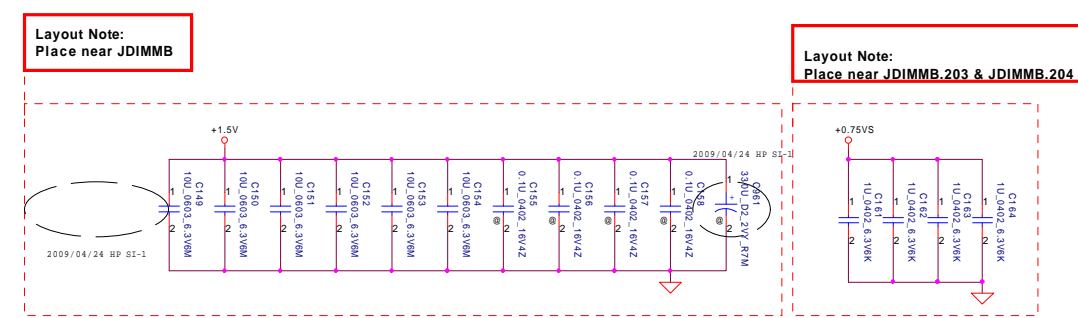
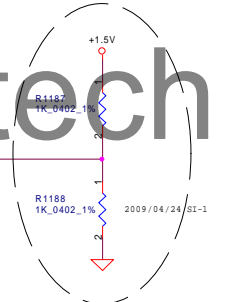


**TOP SLOT**

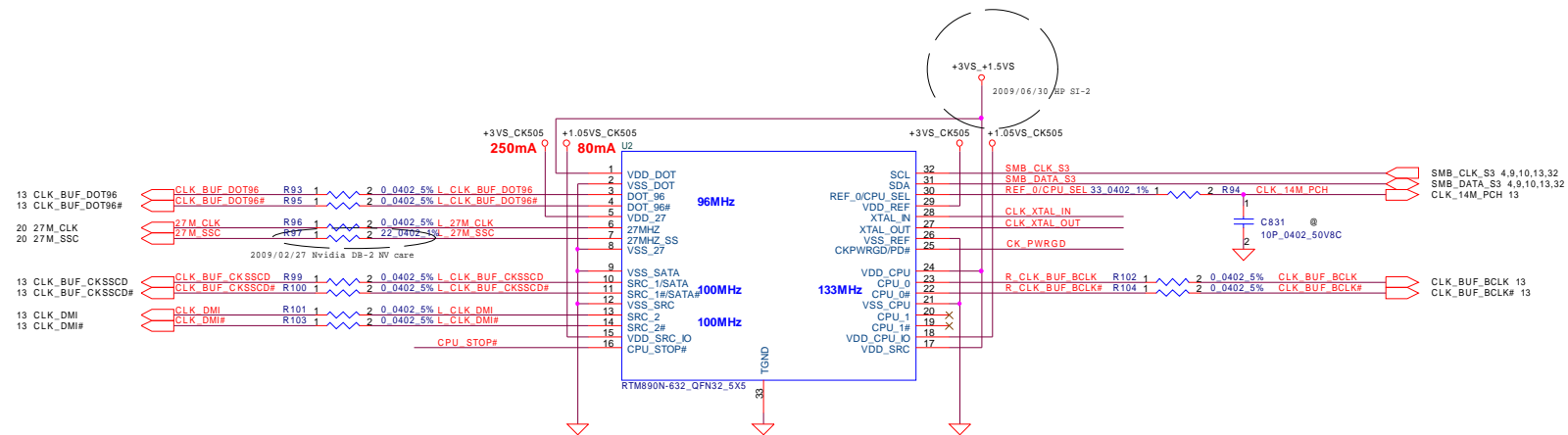
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### For ME/iAMT debug

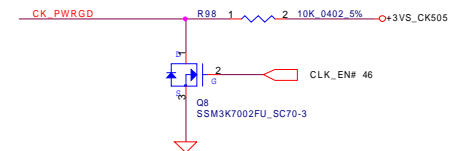
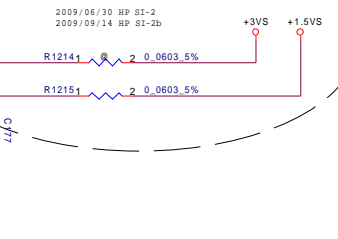
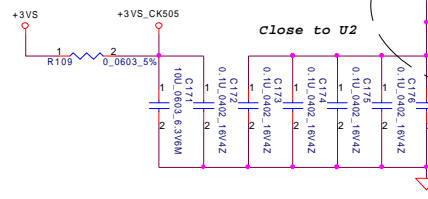
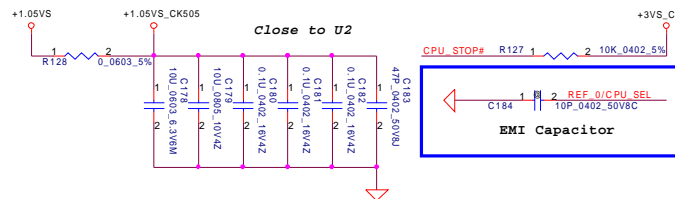
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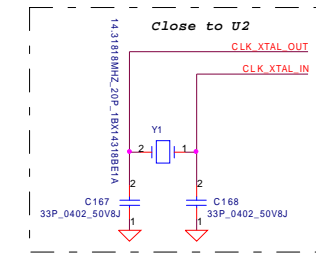
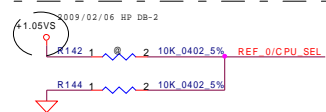
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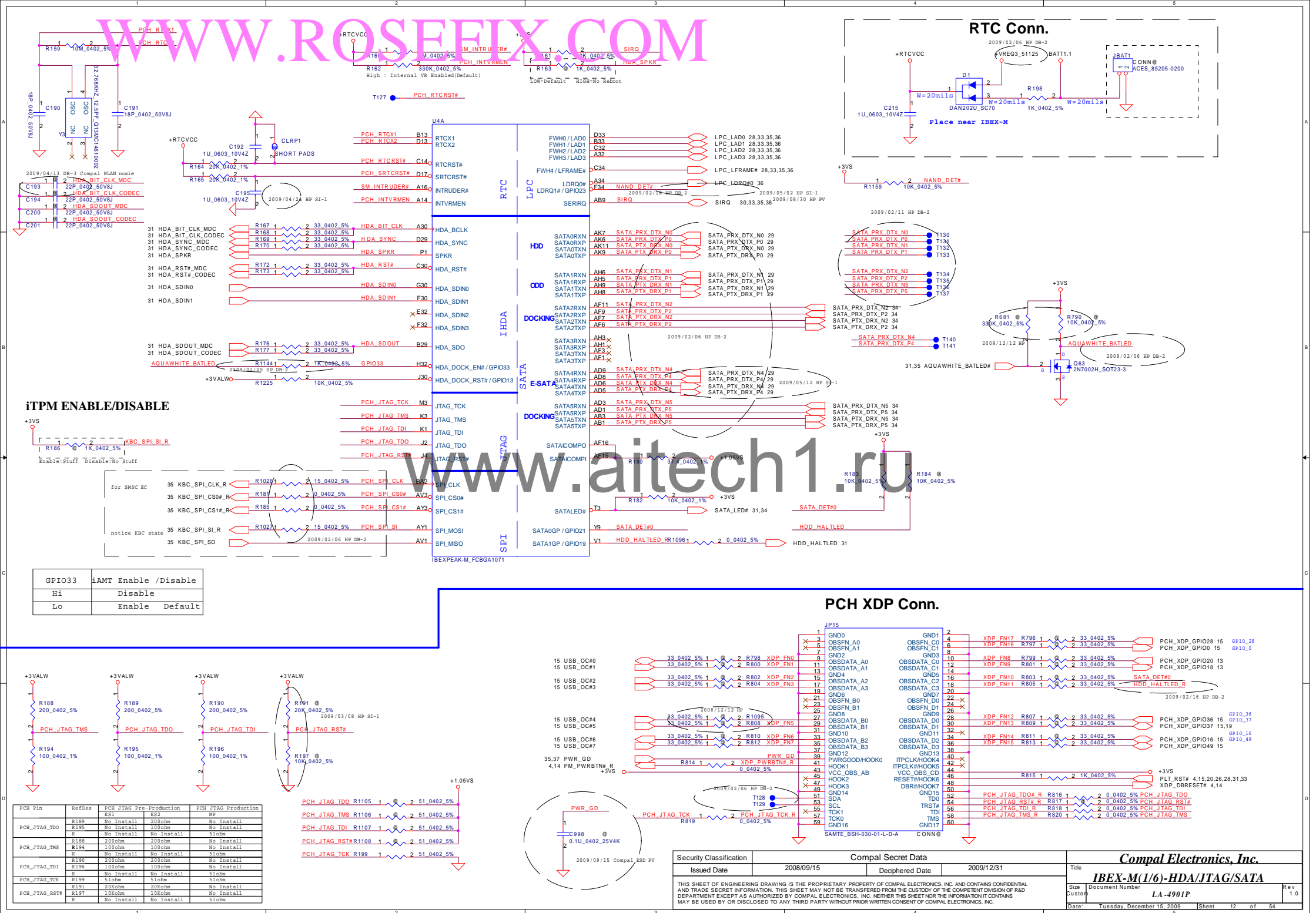


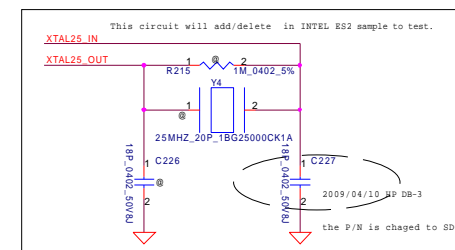
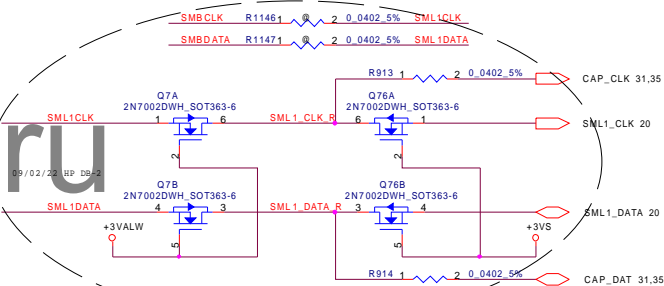
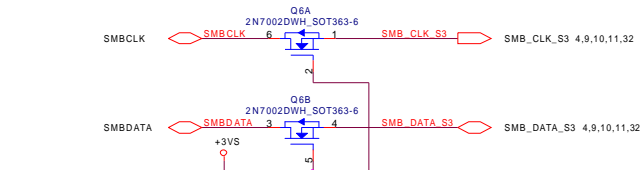
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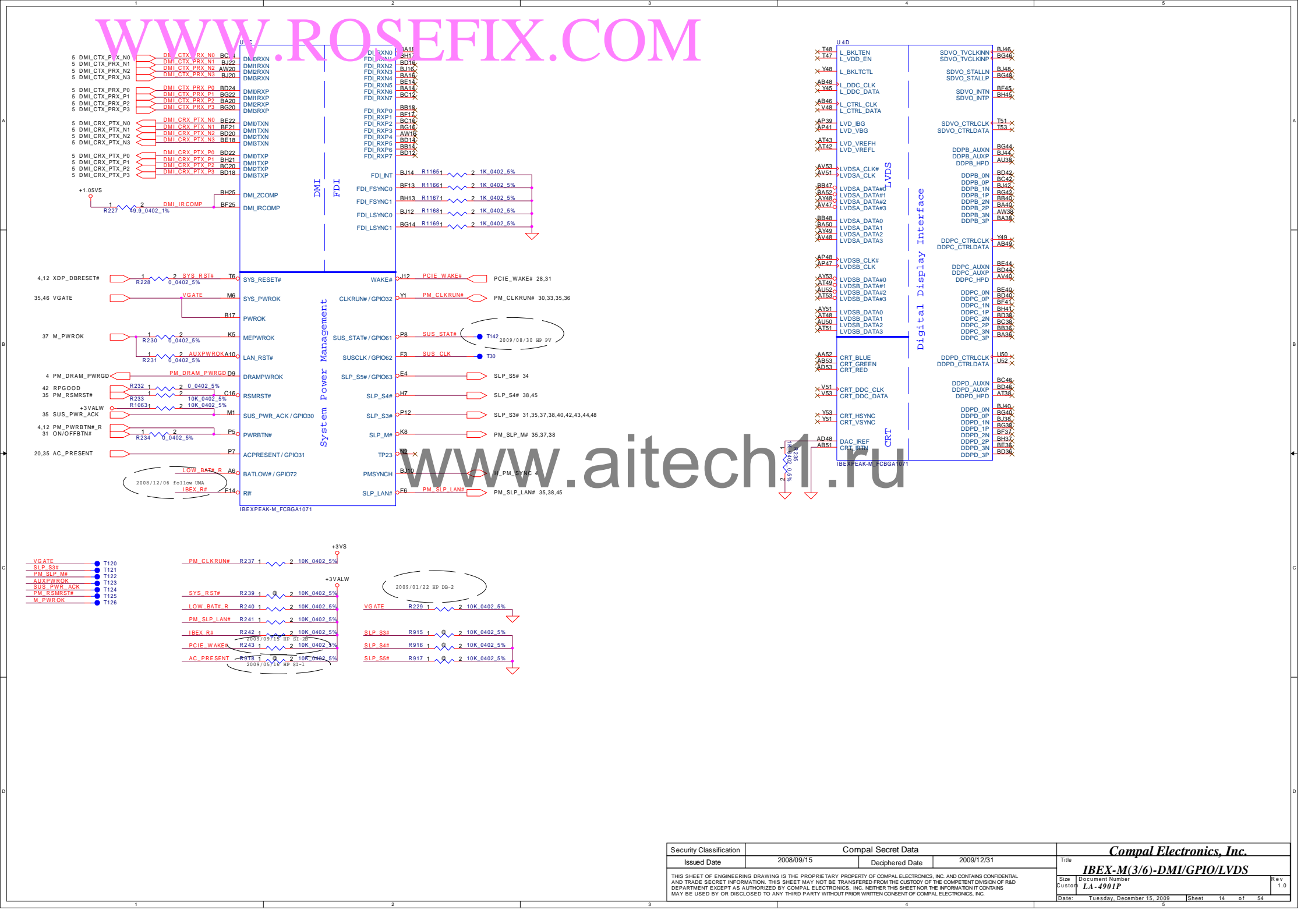
PIN	30	CPU_0	CPU_1
0 (Default)		133MHz	133MHz
1		100MHz	100MHz

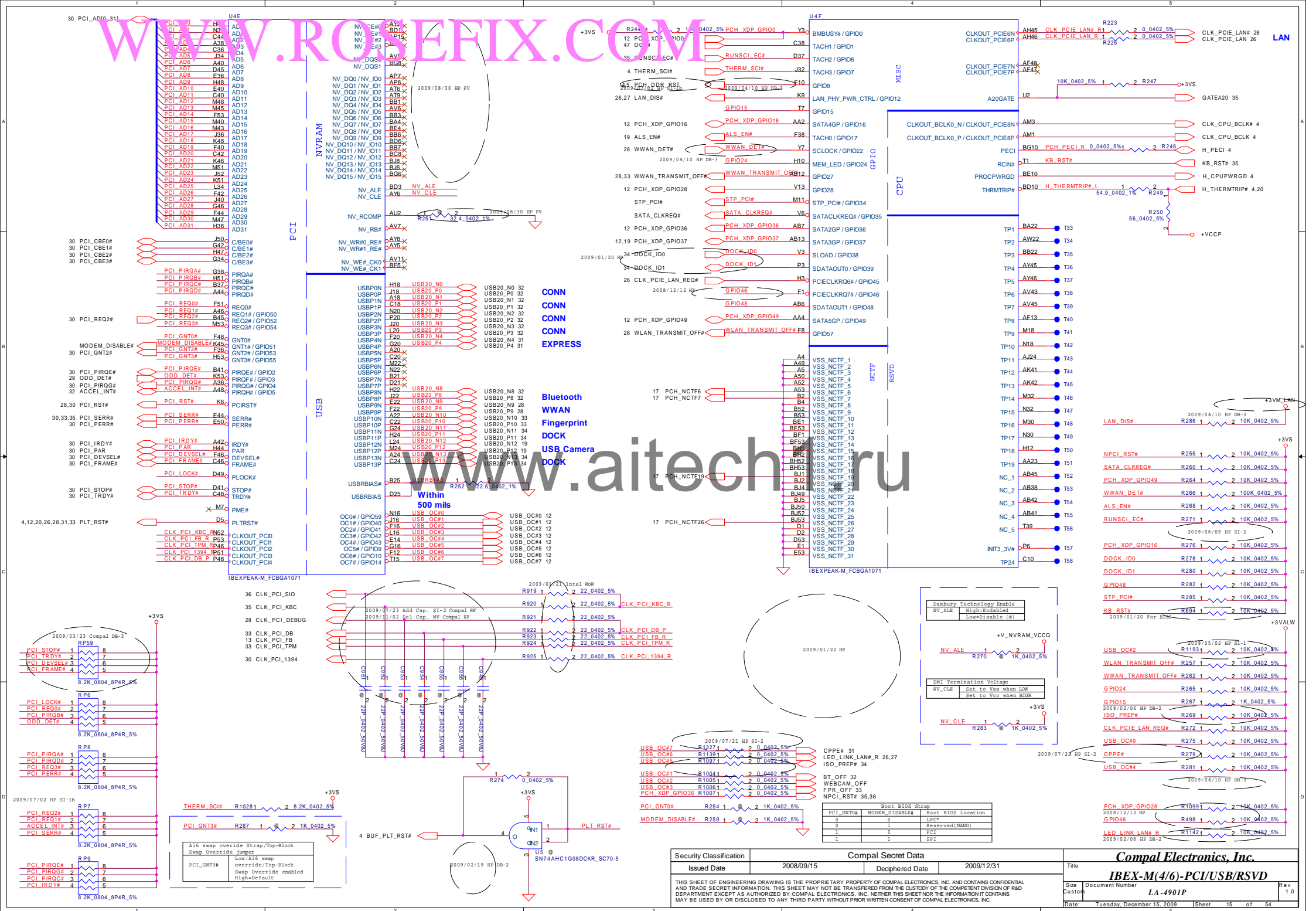


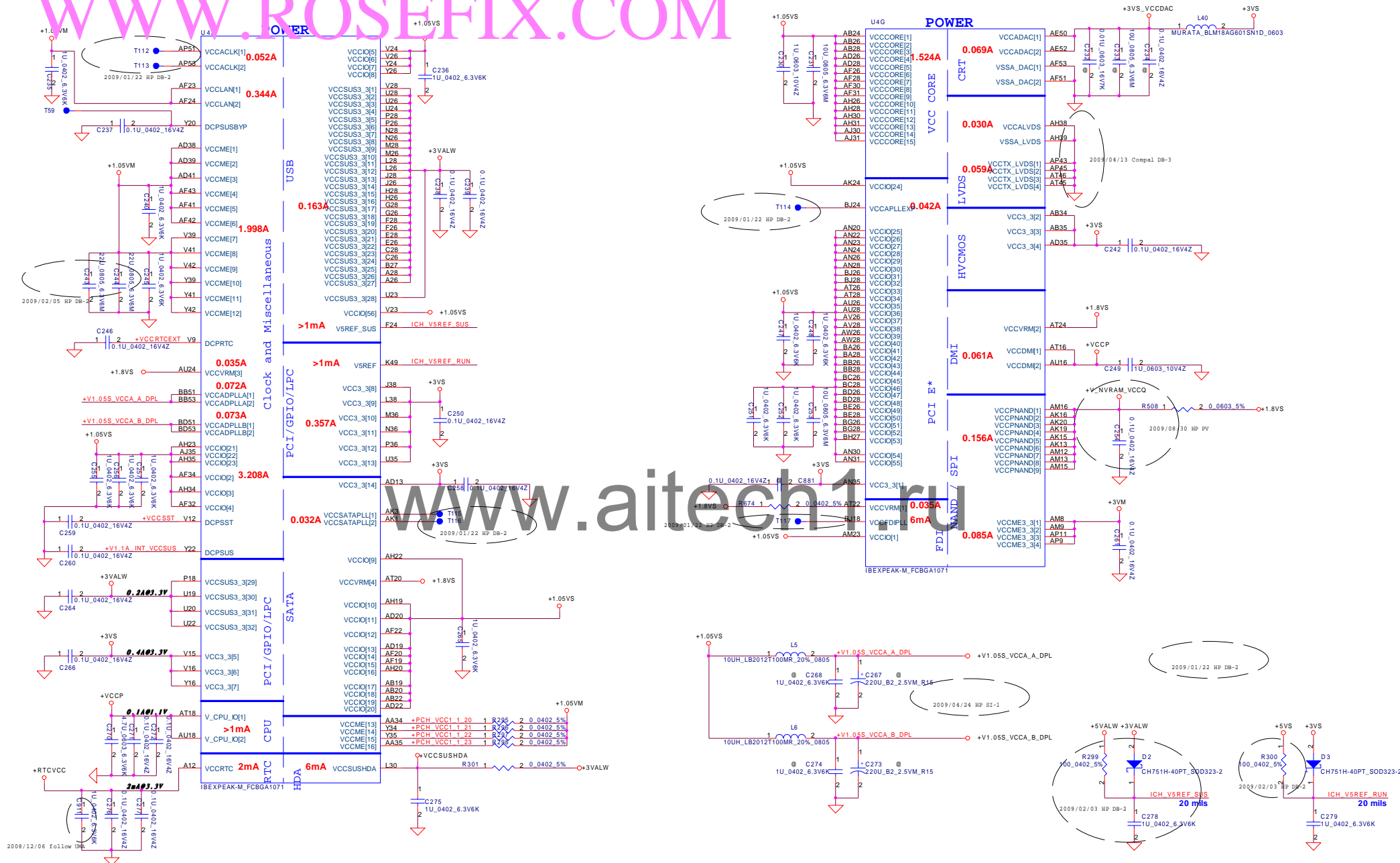




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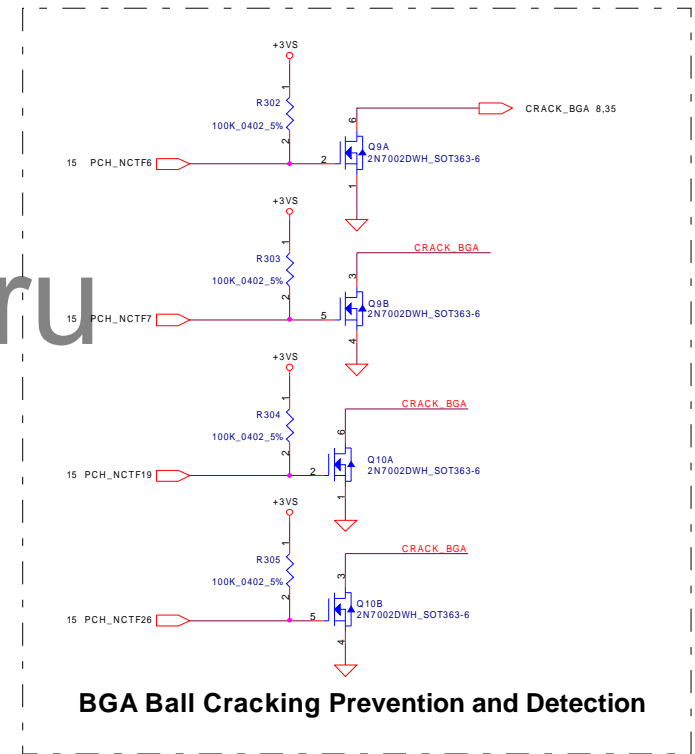




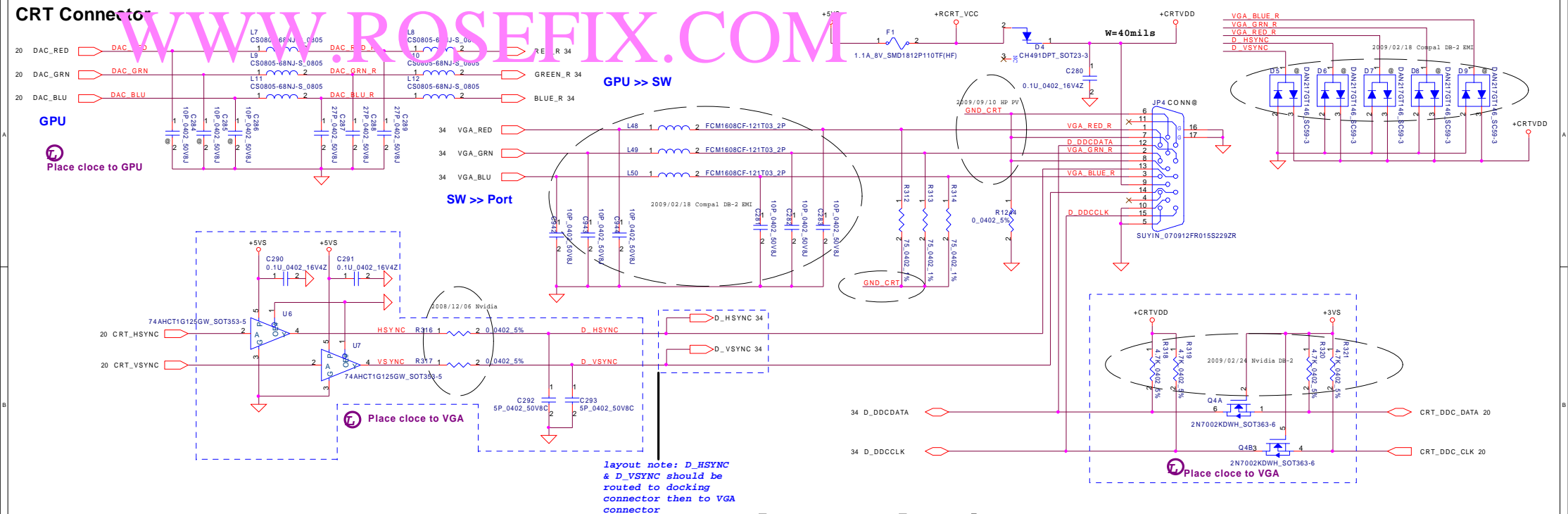


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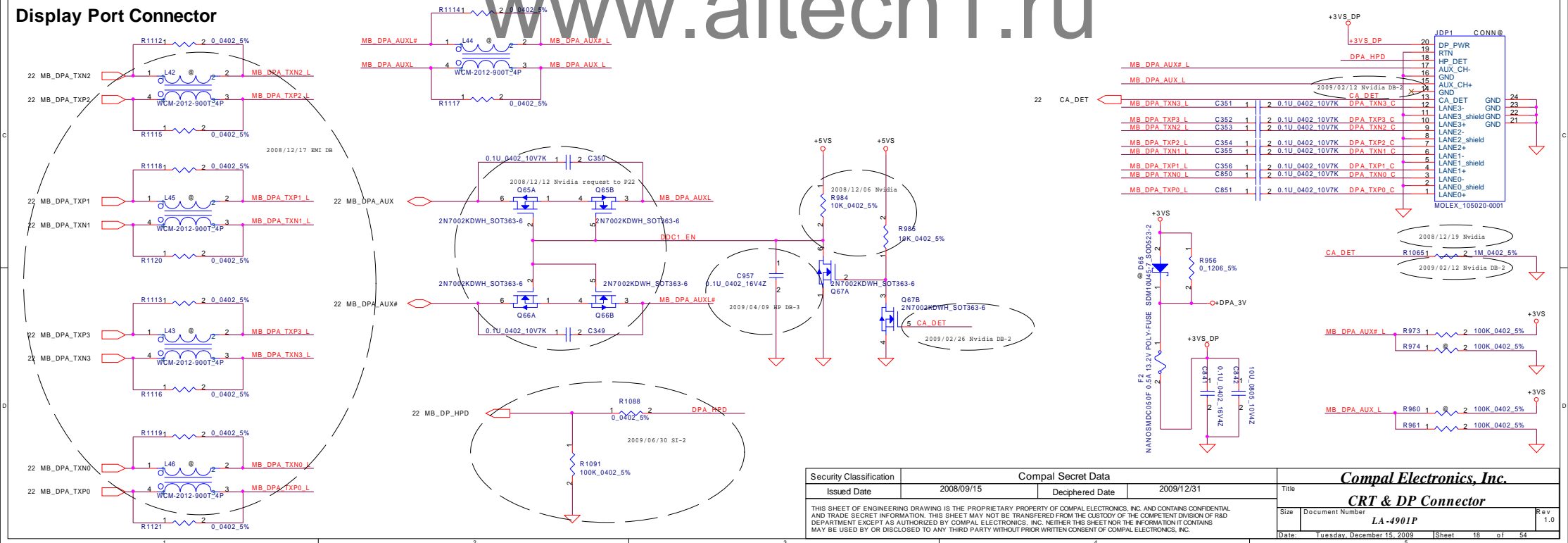
J41		U4	
AY1	VSS[159]	B16	VSS[ ]
B11	VSS[160]	AA19	VSS[1]
B19	VSS[161]	AA20	VSS[2]
B21	VSS[162]	AA22	VSS[3]
B31	VSS[163]	AA19	VSS[4]
B35	VSS[164]	AA24	VSS[5]
B39	VSS[165]	AA26	VSS[6]
B43	VSS[166]	AA28	VSS[7]
B47	VSS[167]	AA30	VSS[8]
B51	VSS[168]	AA31	VSS[9]
B52	VSS[169]	AA32	VSS[10]
B53	VSS[170]	AB1	VSS[11]
BB16	VSS[171]	AB15	VSS[12]
BB20	VSS[172]	AB23	VSS[13]
BB24	VSS[173]	AB30	VSS[14]
BB30	VSS[174]	AB31	VSS[15]
BB34	VSS[175]	AB32	VSS[16]
BB38	VSS[176]	AB39	VSS[17]
BB42	VSS[177]	AB43	VSS[18]
BB49	VSS[178]	AB47	VSS[19]
BB5	VSS[179]	AB5	VSS[20]
BC10	VSS[180]	AB6	VSS[21]
BC14	VSS[181]	AC2	VSS[22]
BC18	VSS[182]	AC52	VSS[23]
BC2	VSS[183]	AD11	VSS[24]
BC22	VSS[184]	AD12	VSS[25]
BC32	VSS[185]	AD16	VSS[26]
BC38	VSS[186]	AD23	VSS[27]
BC40	VSS[187]	AD30	VSS[28]
BC44	VSS[188]	AD31	VSS[29]
BC52	VSS[189]	AD32	VSS[30]
BD5	VSS[190]	AD34	VSS[31]
BD48	VSS[191]	AD42	VSS[32]
BD49	VSS[192]	AD46	VSS[33]
BD5	VSS[193]	AD49	VSS[34]
BE12	VSS[194]	AD7	VSS[35]
BE16	VSS[195]	AE2	VSS[36]
BE20	VSS[196]	AE4	VSS[37]
BE24	VSS[197]	AF12	VSS[38]
BE30	VSS[198]	AF19	VSS[39]
BE34	VSS[199]	AF46	VSS[40]
BE38	VSS[200]	AF47	VSS[41]
BE42	VSS[201]	AF48	VSS[42]
BE46	VSS[202]	AF5	VSS[43]
BE50	VSS[203]	AG2	VSS[44]
BE54	VSS[204]	AG52	VSS[45]
BE58	VSS[205]	AG2	VSS[46]
BE6	VSS[206]	AG52	VSS[47]
BF3	VSS[207]	AH11	VSS[48]
BF49	VSS[208]	AH15	VSS[49]
BF51	VSS[209]	AH16	VSS[50]
BF51	VSS[210]	AH24	VSS[51]
BG24	VSS[211]	AH32	VSS[52]
BG18	VSS[212]	AH33	VSS[53]
BG4	VSS[213]	AH47	VSS[54]
BG50	VSS[214]	AH47	VSS[55]
BH11	VSS[215]	AH47	VSS[56]
BH15	VSS[216]	AH47	VSS[57]
BH23	VSS[217]	AH47	VSS[58]
BH31	VSS[218]	AH47	VSS[59]
BH35	VSS[219]	AH47	VSS[60]
BH39	VSS[220]	AH47	VSS[61]
BH43	VSS[221]	AH47	VSS[62]
BH47	VSS[222]	AH47	VSS[63]
BH7	VSS[223]	AH47	VSS[64]
C12	VSS[224]	AH47	VSS[65]
C12	VSS[225]	AH47	VSS[66]
C50	VSS[226]	AH47	VSS[67]
D51	VSS[227]	AH47	VSS[68]
E12	VSS[228]	AH47	VSS[69]
E16	VSS[229]	AH47	VSS[70]
E20	VSS[230]	AH47	VSS[71]
E24	VSS[231]	AH47	VSS[72]
E30	VSS[232]	AH47	VSS[73]
E34	VSS[233]	AH47	VSS[74]
E38	VSS[234]	AH47	VSS[75]
E42	VSS[235]	AH47	VSS[76]
E46	VSS[236]	AH47	VSS[77]
E48	VSS[237]	AH47	VSS[78]
E6	VSS[238]	AH47	VSS[79]
F8	VSS[239]	AH47	VSS[80]
F49	VSS[240]	AH47	VSS[81]
F5	VSS[241]	AH47	VSS[82]
G10	VSS[242]	AH47	VSS[83]
G18	VSS[243]	AH47	VSS[84]
G2	VSS[244]	AH47	VSS[85]
G22	VSS[245]	AH47	VSS[86]
G32	VSS[246]	AH47	VSS[87]
G36	VSS[247]	AH47	VSS[88]
G40	VSS[248]	AH47	VSS[89]
G44	VSS[249]	AH47	VSS[90]
G52	VSS[250]	AH47	VSS[91]
AF39	VSS[251]	AH47	VSS[92]
H16	VSS[252]	AH47	VSS[93]
H20	VSS[253]	AH47	VSS[94]
H30	VSS[254]	AH47	VSS[95]
H34	VSS[255]	AH47	VSS[96]
H38	VSS[256]	AH47	VSS[97]
H42	VSS[257]	AH47	VSS[98]
H42	VSS[258]	AH47	VSS[99]

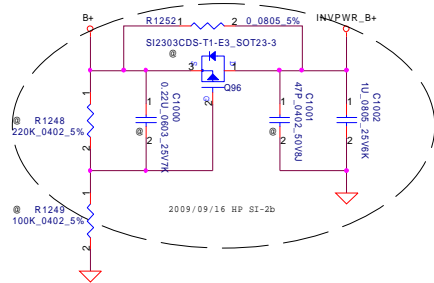
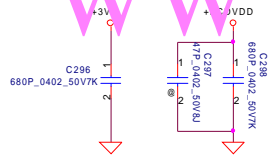


## CRT Connector

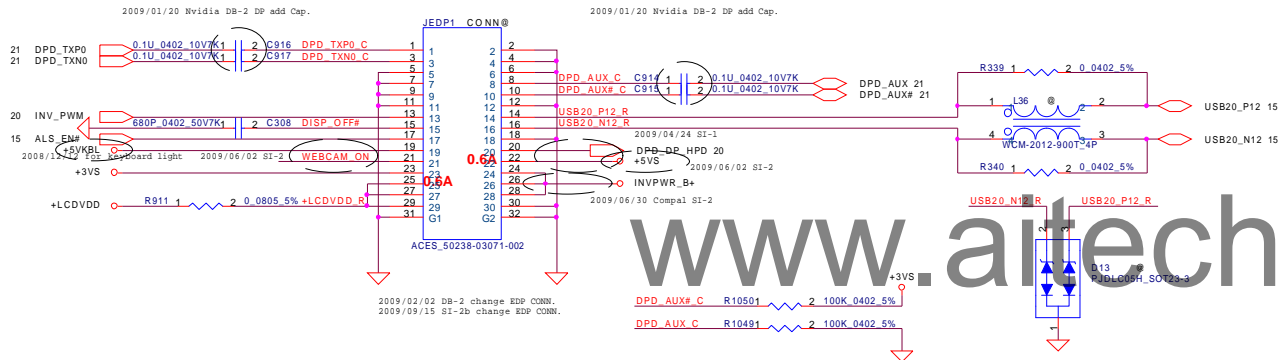
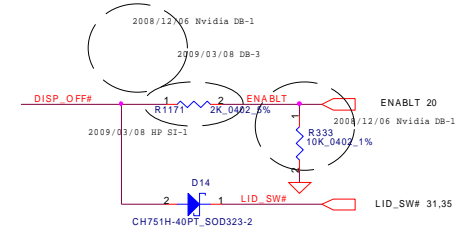
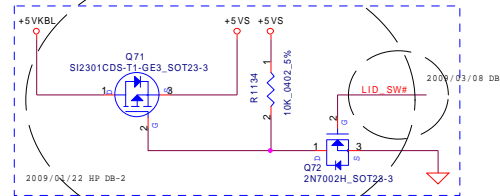


### Display Port Connector

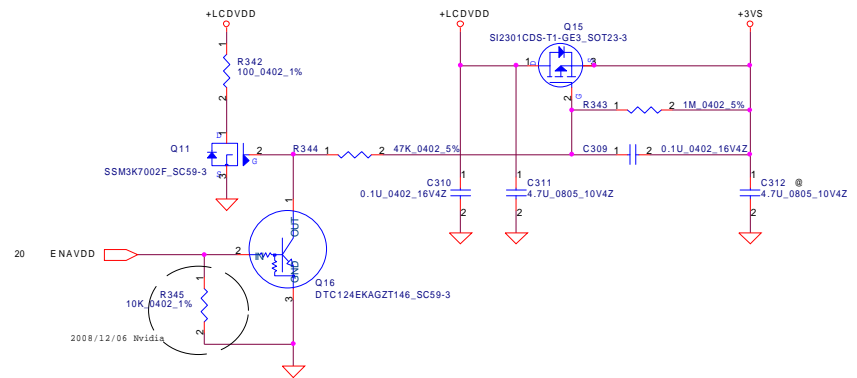




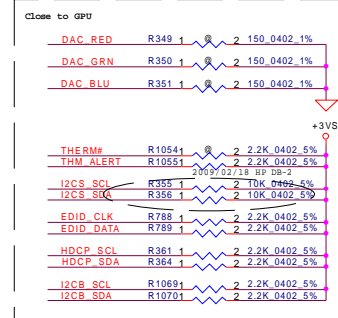
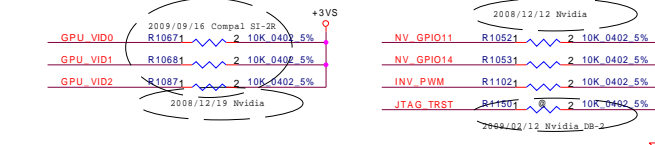
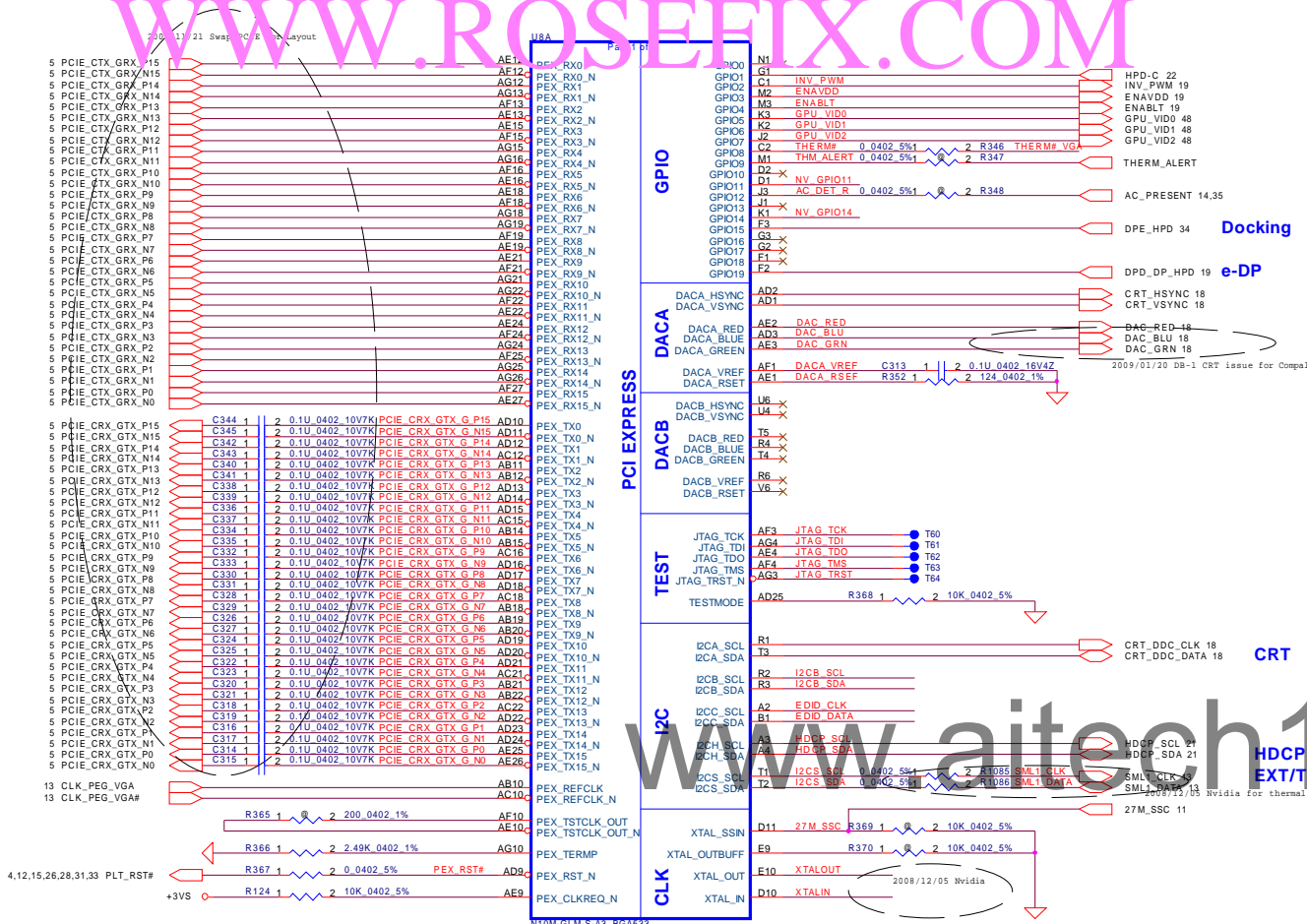
### Key\_Board\_Light power Control



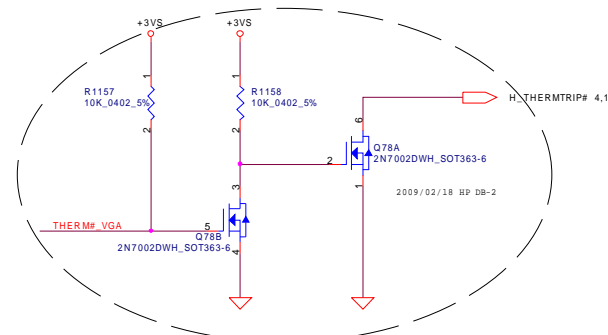
### LCD POWER CIRCUIT



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GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	HPD-C (used for IFPC)
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	NVVDD VID2
GPIO8	IN	L	OVERT
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT	N/A	MEM_VREF
GPIO11	OUT	L	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	MEM_VID
GPIO14	OUT	H	PS Control
GPIO15	IN	N/A	HPD-E (used for IFPE)
GPIO16	OUT	N/A	FAN PWM Control
GPIO17		N/A	
GPIO18		N/A	
GPIO19	IN	N/A	HPD-D (used for IFPD)



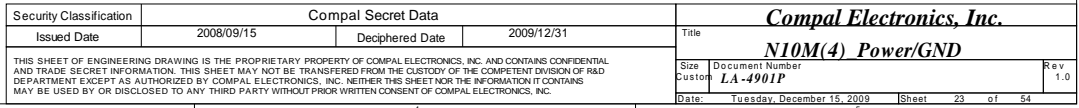


Stuff R394 --> N10M-GLM, N10M-NS  
 Stuff R402 --> N10M-NS  
 Stuff R403 --> N10M-GLM

R402/R403:  
- 15K: VBIOS combined in SBIOS  
- 35K: use VBIOS rom chip

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b><i>N10M(2) LVDS&amp;DP&amp;HDCP</i></b>	
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				Custom	1
				Document Number	
				LA-4901P	
				Date: Tuesday, December 15, 2009	Sheet 21 of 54





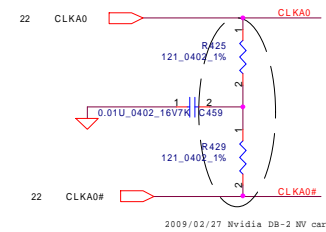
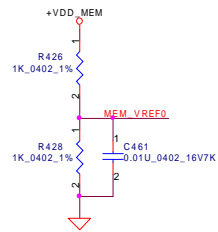
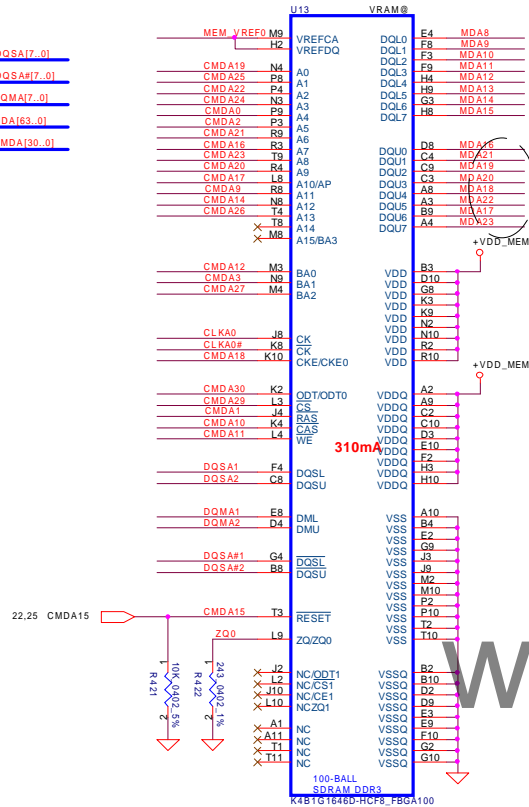
# VRAM LD R3 chips (512 MB)

64Mx16 DDI 3, 00MHz, 2\*4 ==>512MB

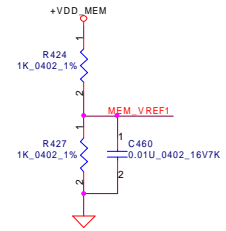
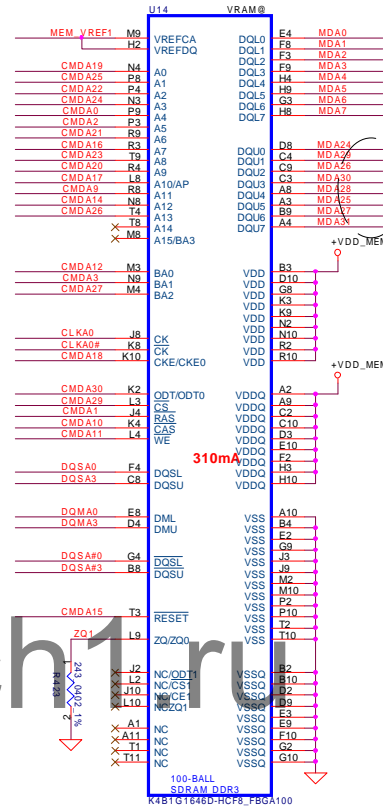
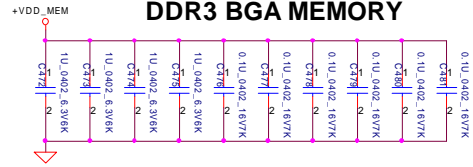
Low 32 bit FB

yn : (5TQ GCBFR-2C-->S/ 000033/00  
ansur : K4V1G16460-HC12-->SA00 03570

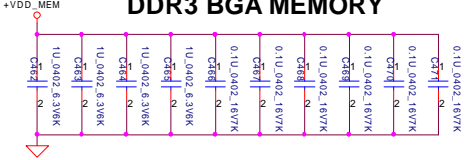
22.25 DQSA[7..0] DQSA[7..0]  
22.25 DQSA[7..0] DQSA[7..0]  
22.25 DQMA[7..0] DQMA[7..0]  
22.25 MDA[63..0] MDA[63..0]  
22.25 CMDA[30..0] CMDA[30..0]



## DDR3 BGA MEMORY



## DDR3 BGA MEMORY



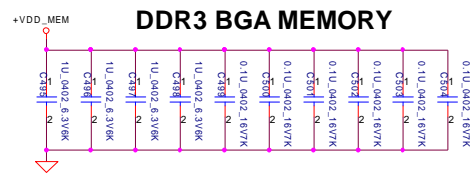
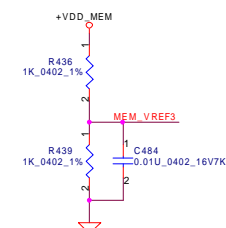
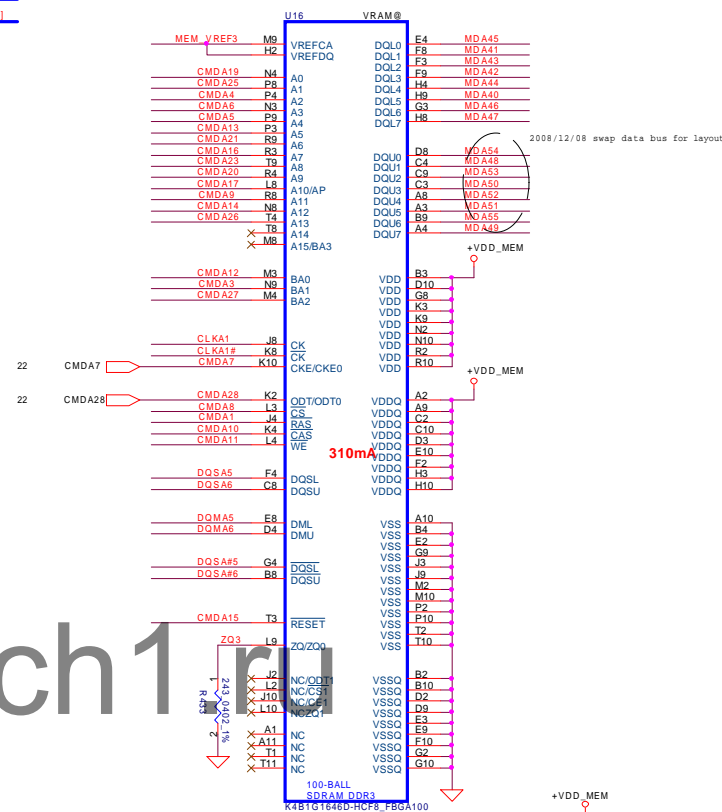
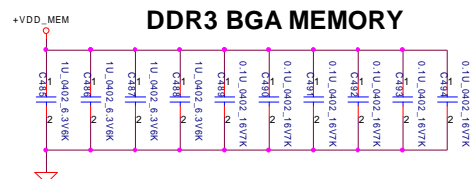
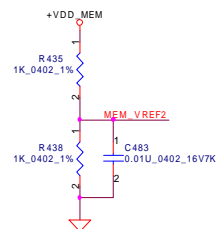
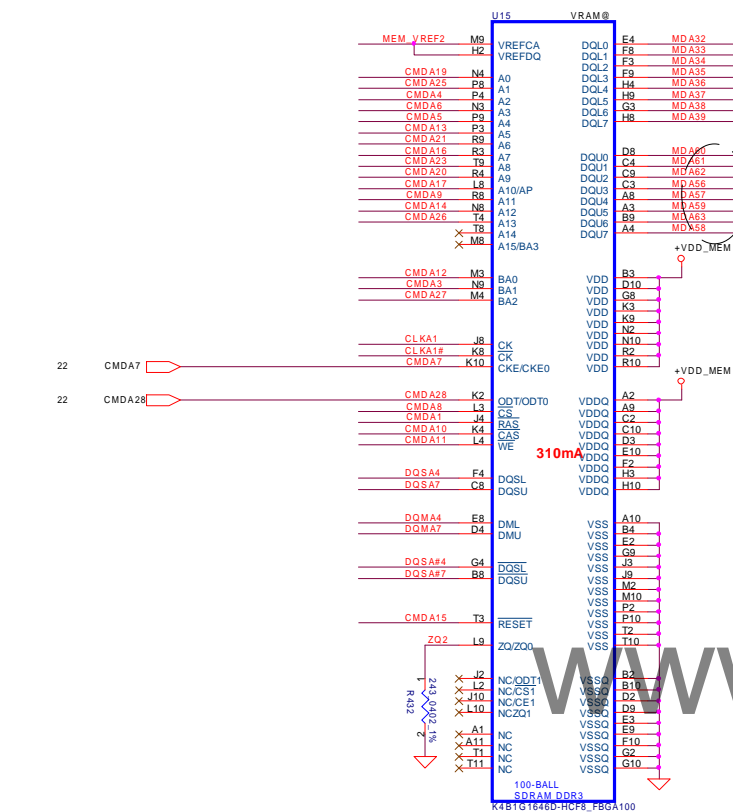
DATA Bus		
Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4	A2	
CMD5	A4	
CMD6	A3	
CMD7	CKE	
CMD8	CS#	
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	

LOW HIGH

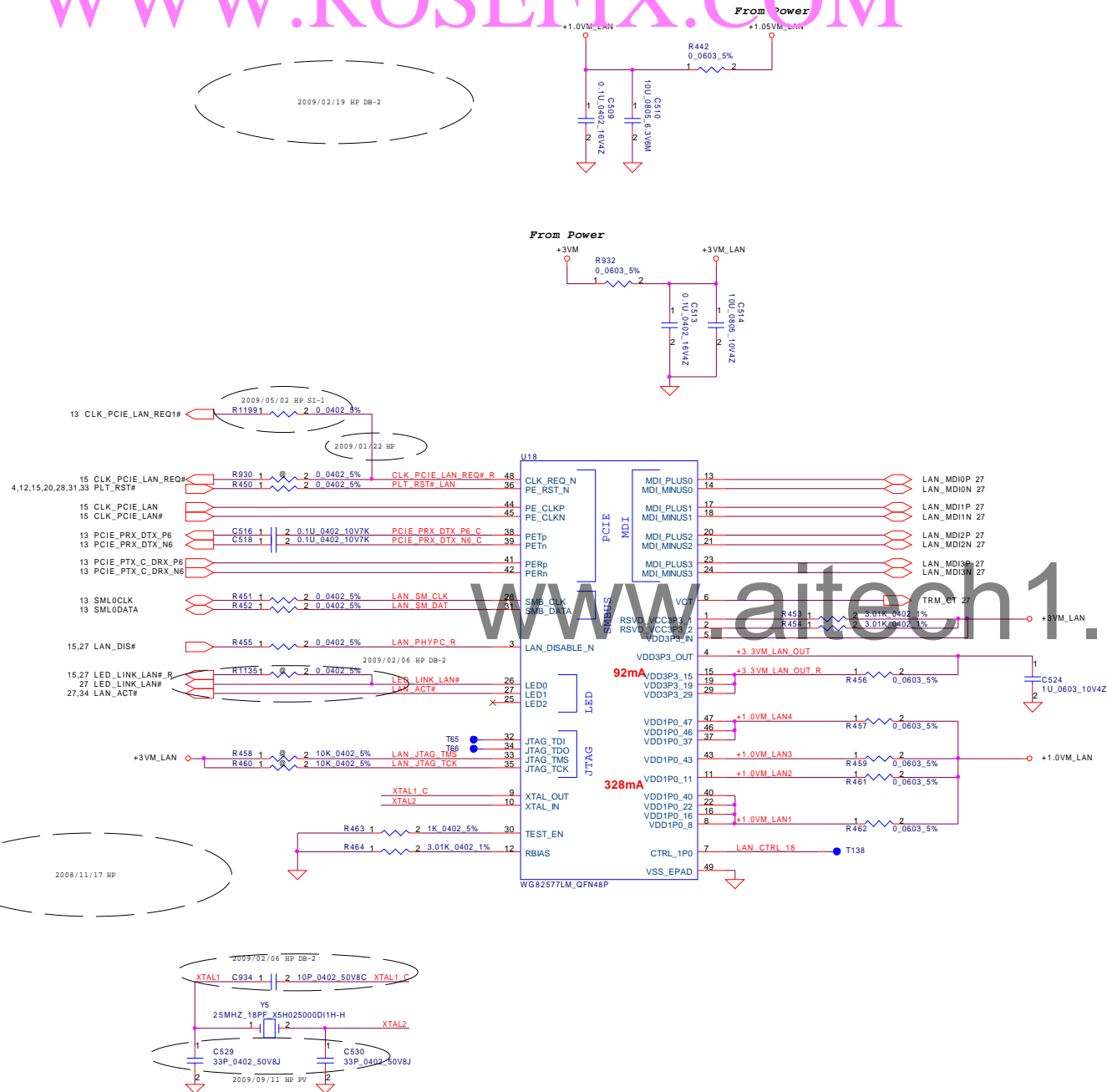
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	VRAM DDR3
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				LA-4901P	
				Date	Tuesday, December 15, 2009
				Sheet	24 of 54

**High 32 bit FB**

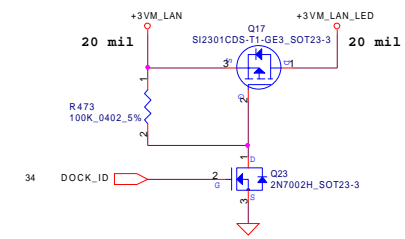
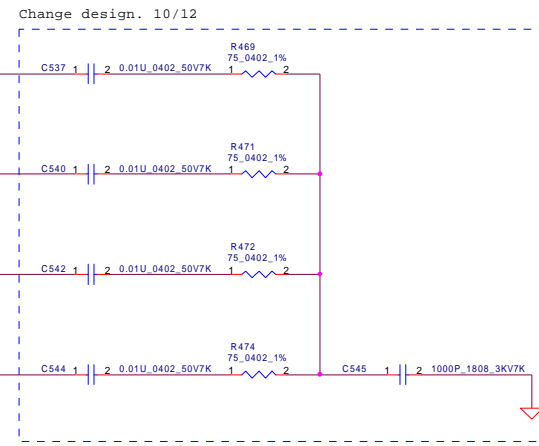
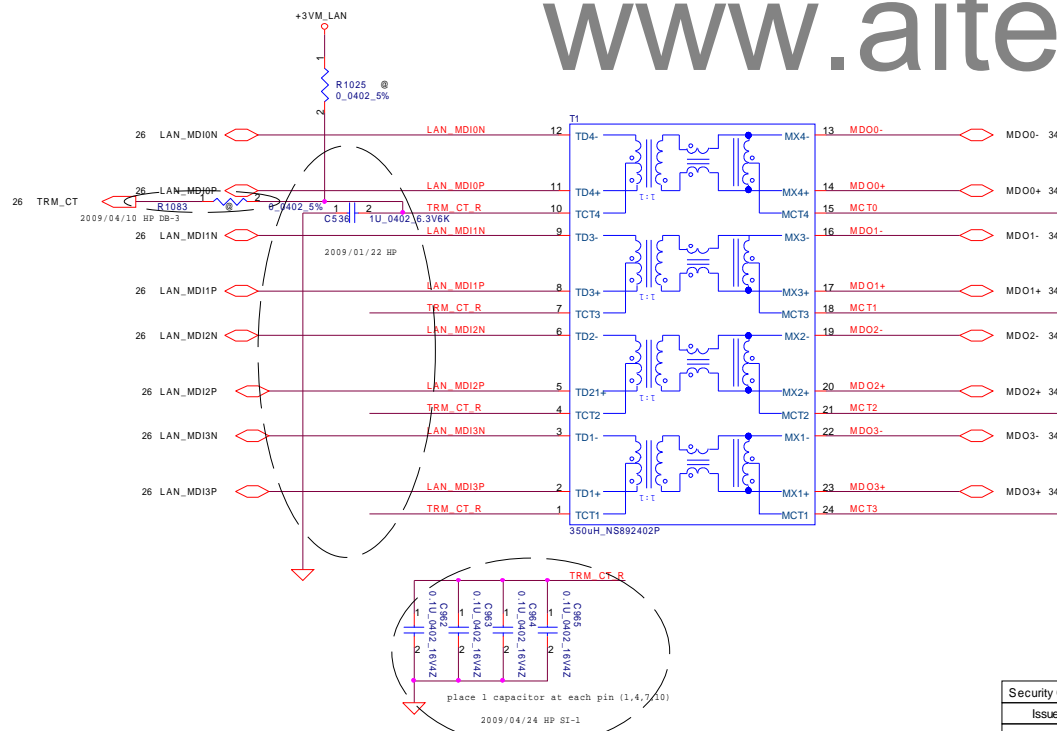
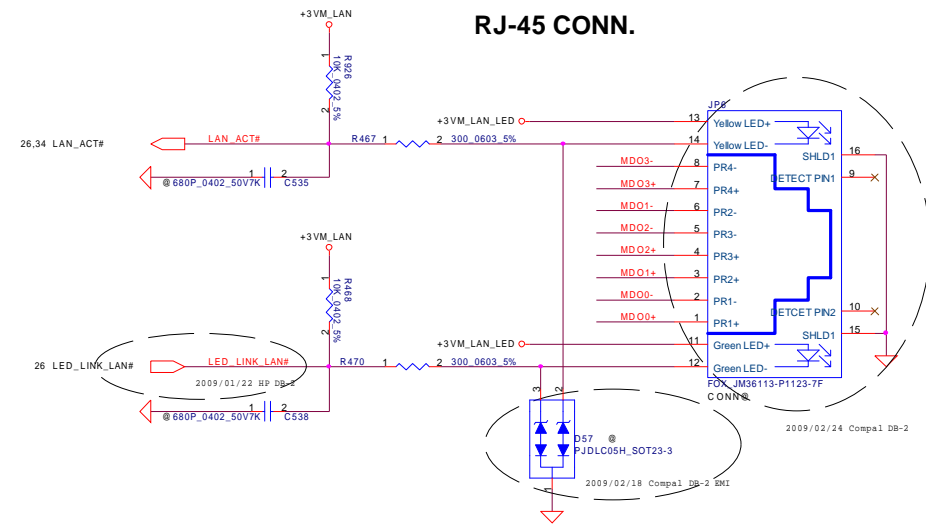
22,24	DC	A[7..0]	<input type="checkbox"/>	DC	A[7..0]
22,24	DC	A# [7..0]	<input type="checkbox"/>	DC	A# [7..0]
22,24	DQM	A[7..0]	<input checked="" type="checkbox"/>	DQM	A[7..0]
22,24	MDA	[63..0]	<input type="checkbox"/>	MDA	[63..0]
22,24	CMDA	[30..0]	<input checked="" type="checkbox"/>	CMDA	[30..0]



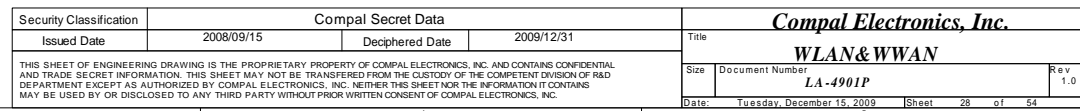
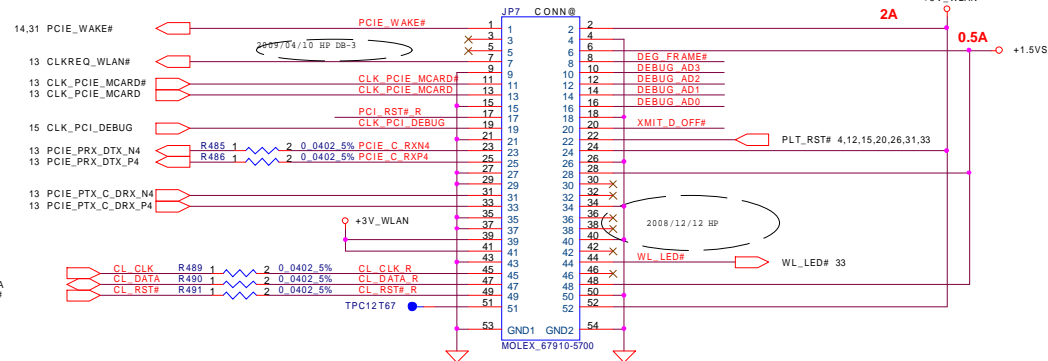
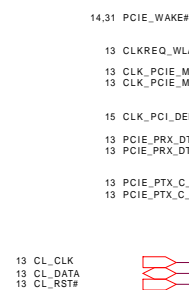
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	VRAM DDR3	
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				Cartier DIS		0.1
				Date:	Tuesday, December 15, 2009	Sheet



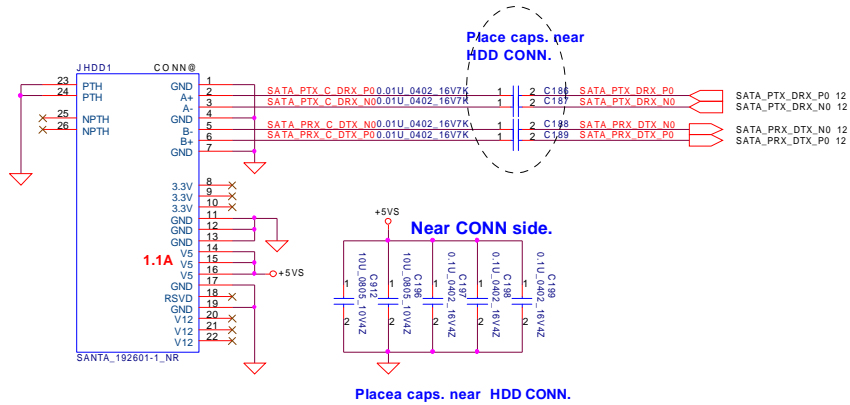
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title		
				Intel 82566 Nineveh		
				Size	Document Number	Rev
					LA-4901P	1.0
				Date:	Tuesday, December 15, 2009	Sheet 26 of 54



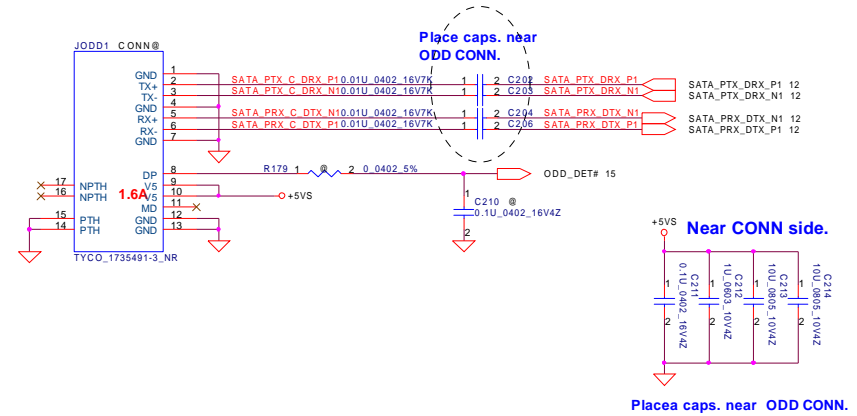
www.aitech1.ru



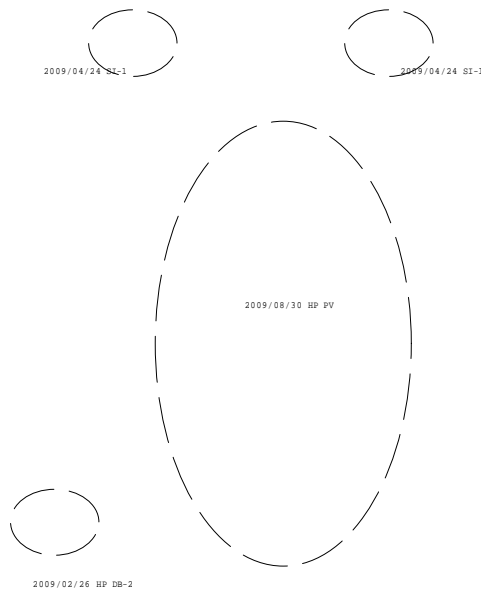
## SATA HDD CONN.



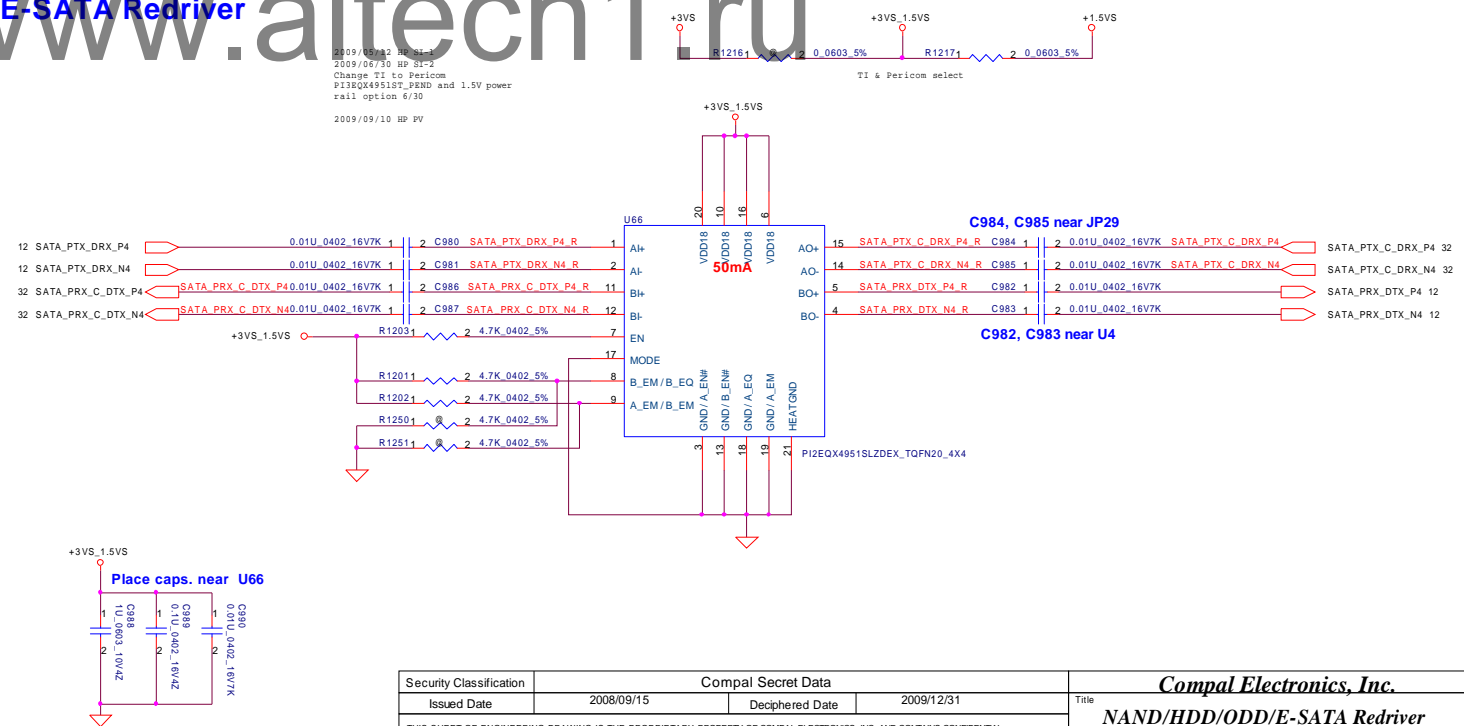
## SATA ODD CONN.



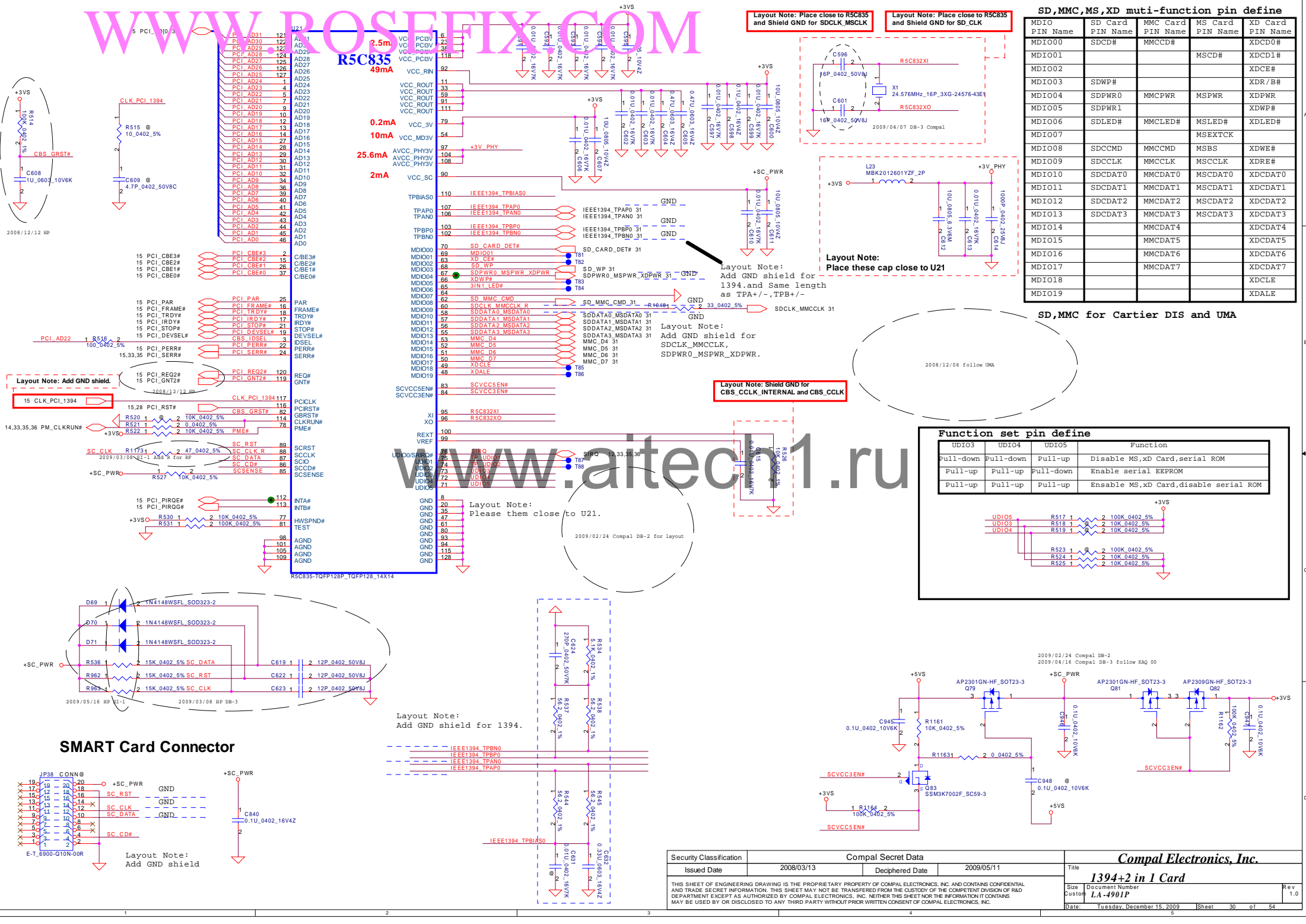
## NAND FLASH



## E-SATA Redriver



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Issued Date	2008/09/15	Deciphered Date	2009/12/31	NAND/HDD/ODD/E-SATA Redriver	
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				Date	Tuesday, December 15, 2009
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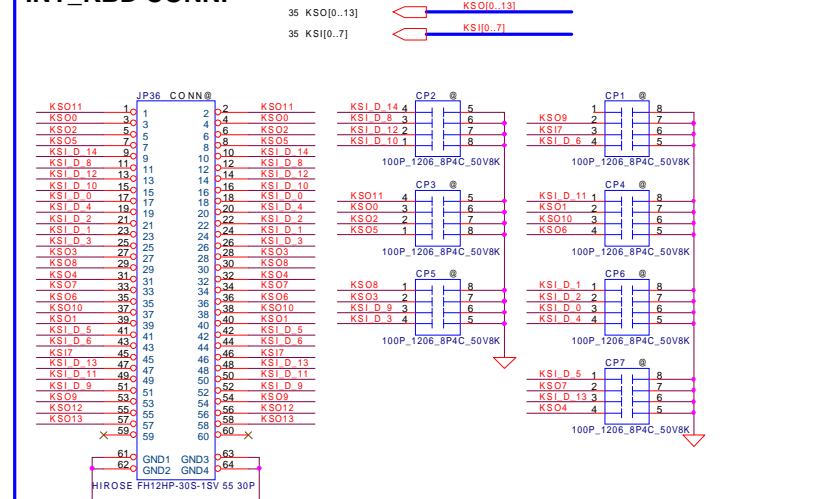
SD, MMC, MS, SD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO0	SDCD#	MMCCD#	MSCD#	XDCD0#
MDIO01				XDCD1#
MDIO02				XDCD2#
MDIO03	SDWP#	MMCPWR	MSPWR	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1			XDPWR
MDIO06	SDLED#	MMCLD#	MSLED#	XDLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14		MMCDAT4		XDCDAT4
MDIO15		MMCDAT5		XDCDAT5
MDIO16		MMCDAT6		XDCDAT6
MDIO17		MMCDAT7		XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

SD, MMC for Cartier DIS and UMA

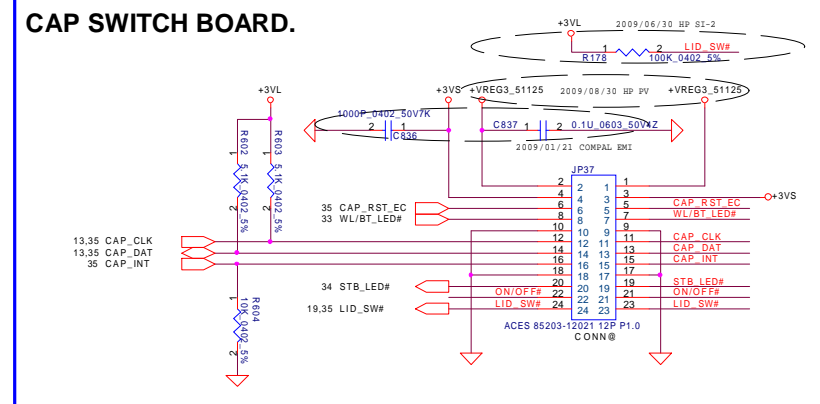
Function set pin define

UDIO3	UDIO4	UDIO5	Function
Pull-down	Pull-down	Pull-up	Disable MS, XD Card, serial ROM
Pull-up	Pull-up	Pull-down	Enable serial EEPROM
Pull-up	Pull-up	Pull-up	Enable MS, XD Card, disable serial ROM

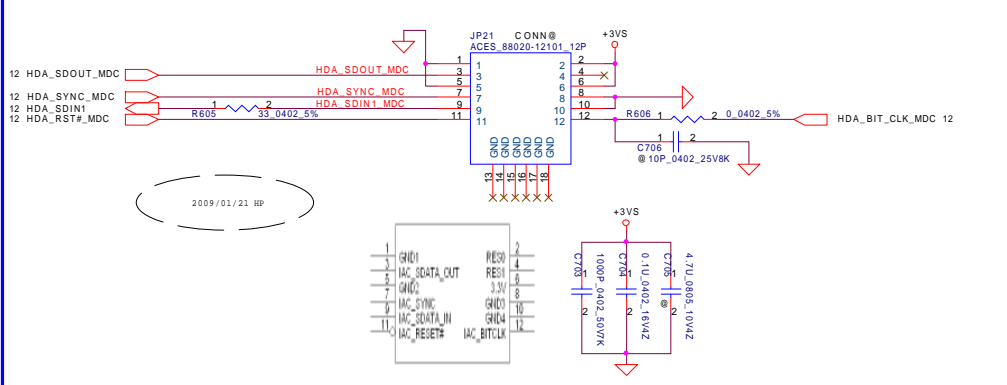


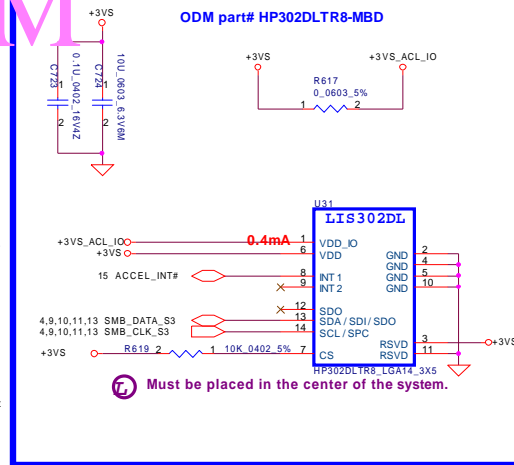
The diagram illustrates the connection of four KSIO signals to the DAP202U\_SOT323-3 component. The signals are KSIO, KSII, KSII, and KSII6. The component is labeled DAP202U\_SOT323-3. The signals are connected to pins D24, D26, D28, and D29. The connections are as follows:

- KSIO (pin 1) is connected to pin D24 (pin 2) and pin D26 (pin 3).
- KSII (pin 1) is connected to pin D26 (pin 2) and pin D28 (pin 3).
- KSII (pin 1) is connected to pin D28 (pin 2) and pin D29 (pin 3).
- KSII6 (pin 1) is connected to pin D29 (pin 2) and pin D29 (pin 3).



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			Size	Document Number	Rev
				LA-4901P	
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JP26

70mA

1  
2  
3  
4  
5

USB20\_P8\_R R611 1 2 0 0.402 5%  
USB20\_N8\_R R612 1 2 0 0.402 5%

ACES\_87Z12-05G0\_5P  
CONN @

+3VALW

BT\_OFF

R614 10K\_0402\_5%  
R615 220K\_0402\_1%

Q33 SI2301CDS-T1-GE3\_SOT23-3

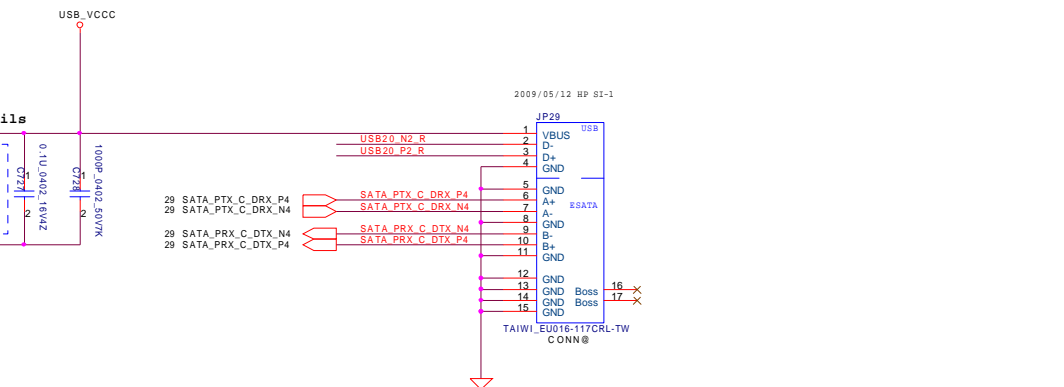
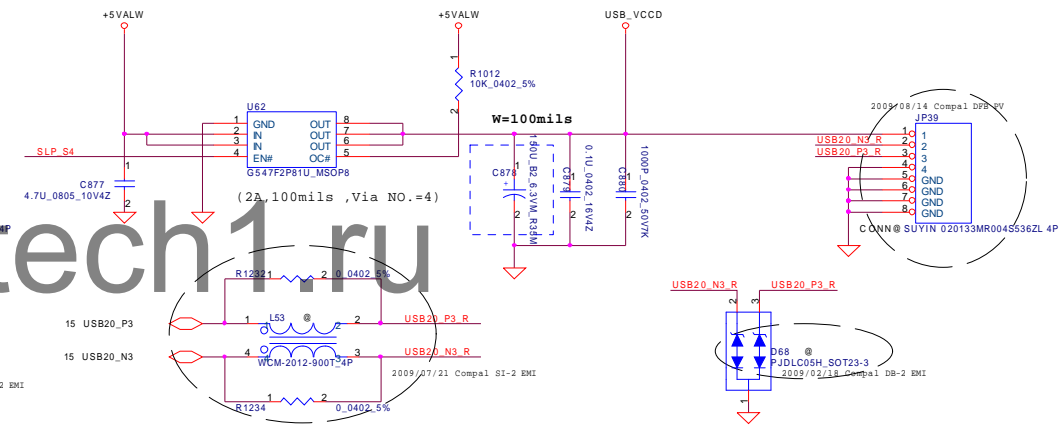
Q33 SSM3K7002FU\_SOT23-3

2009/09/03 Compal PV

+3VAUX\_BT

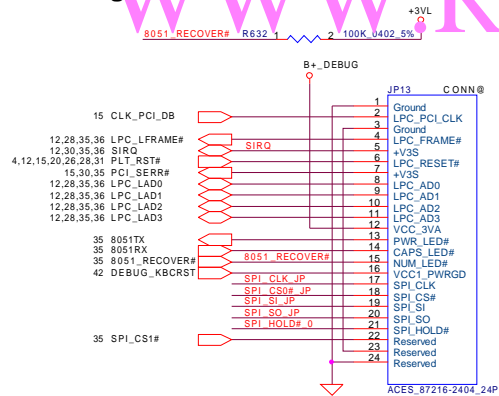
USB20\_P8 15  
USB20\_N8 15  
BT\_LED 33

C716 0.1u/0050\_10WVZ  
C717 0.1u/0402\_16WVZ

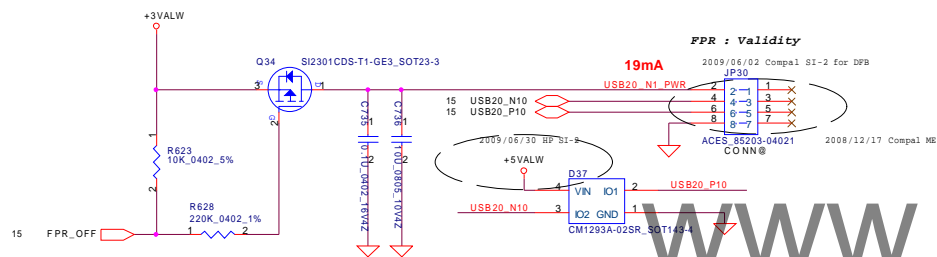


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					LA-4901P	1.0
				Date:	Tuesday, December 15, 2009	Sheet 32 of 54

# LPC Debug Port

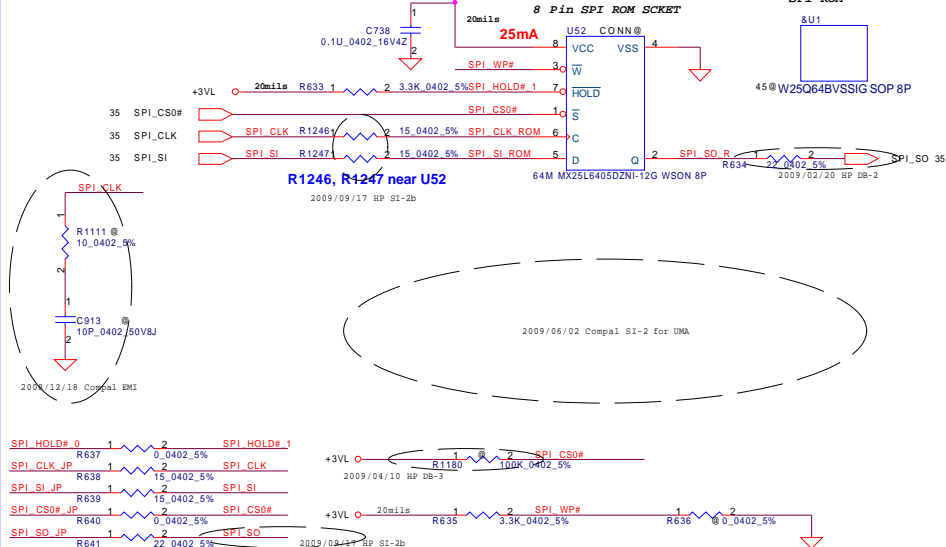


# Finger Printer

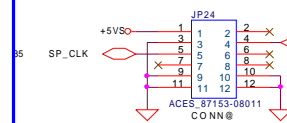


# BIOS ROM(16MB)

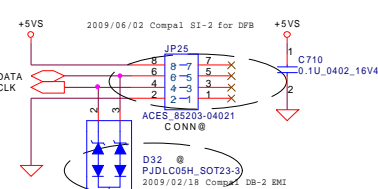
8MB SPI ROM



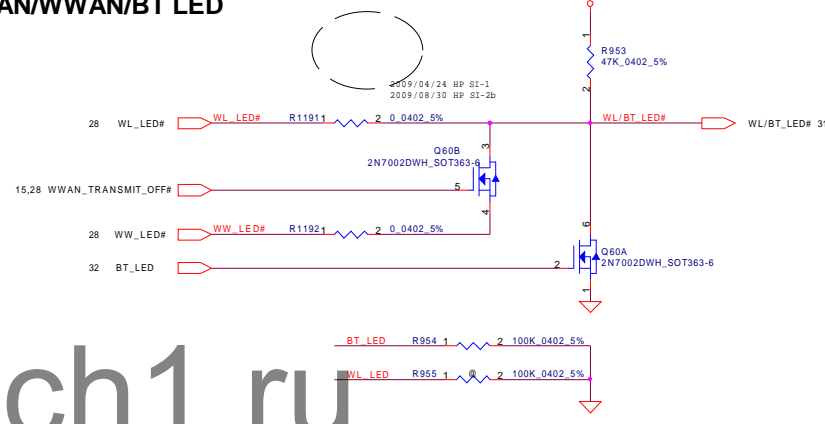
# TrackPoint CONN.



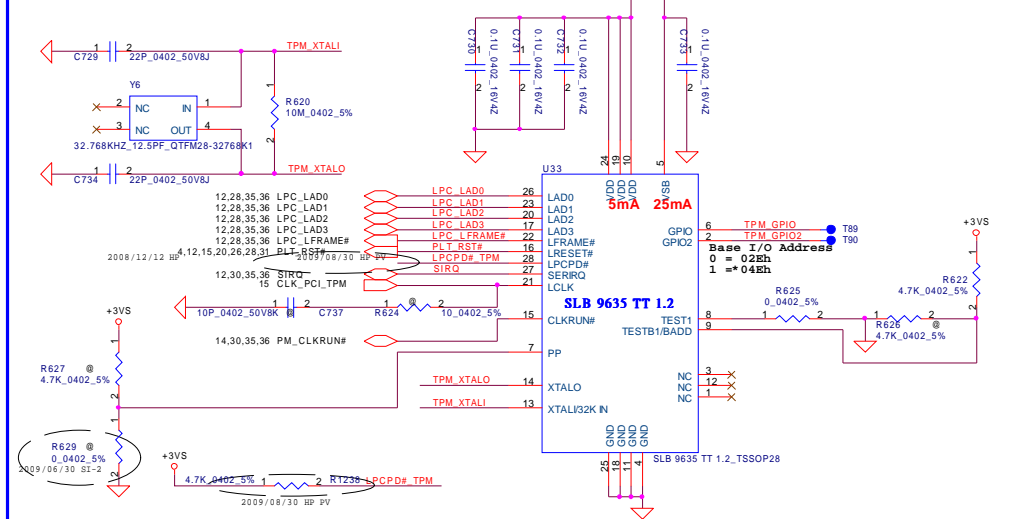
# T/P CONN.



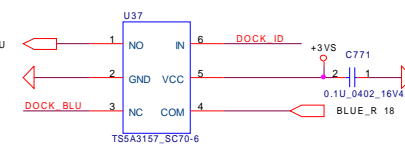
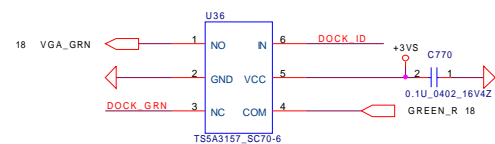
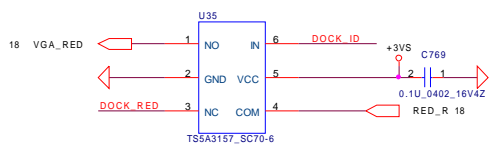
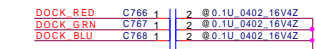
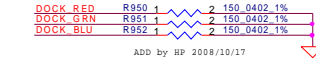
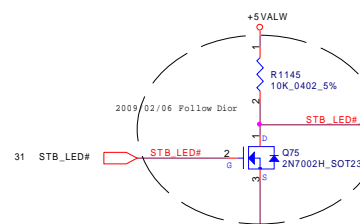
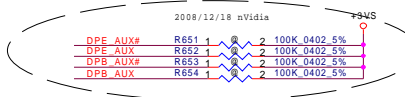
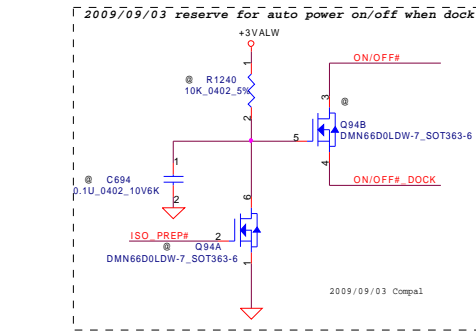
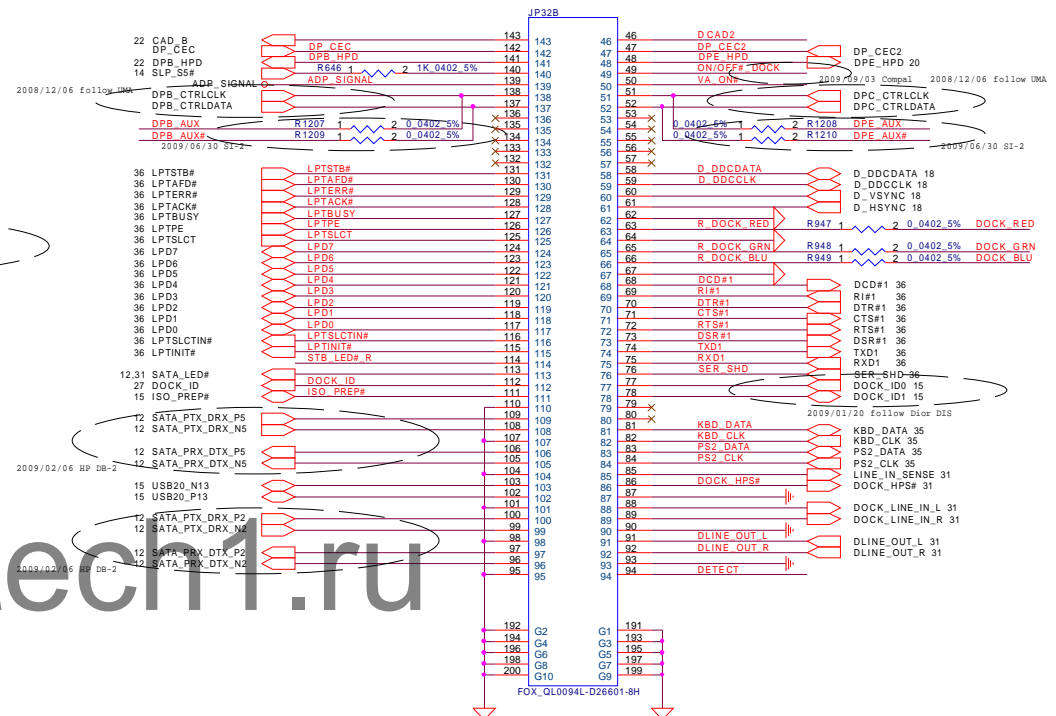
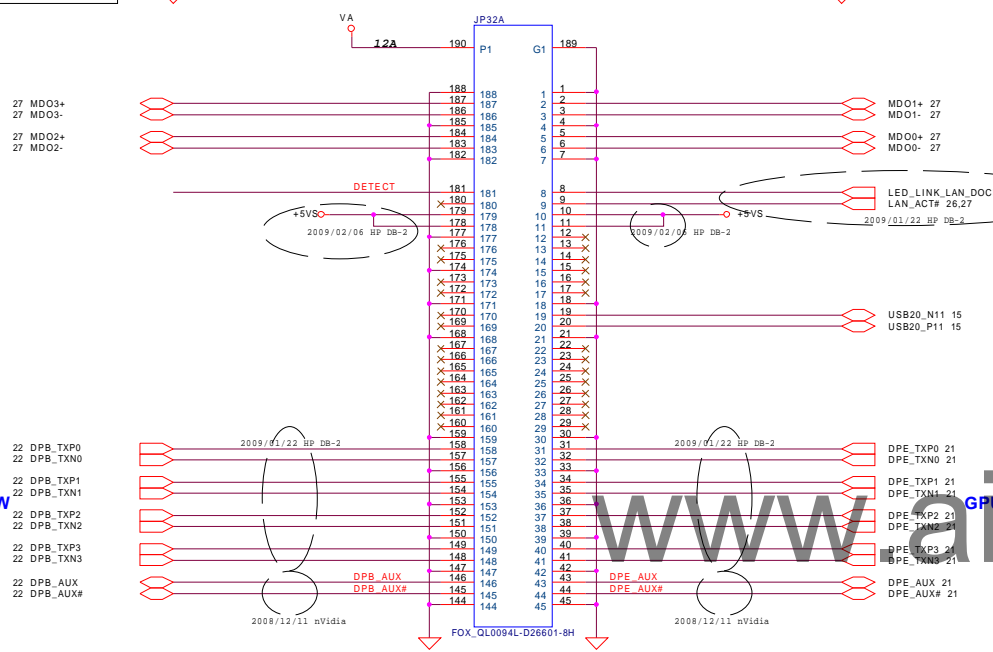
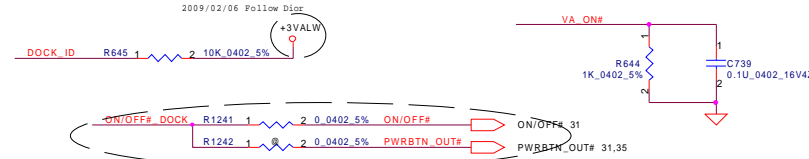
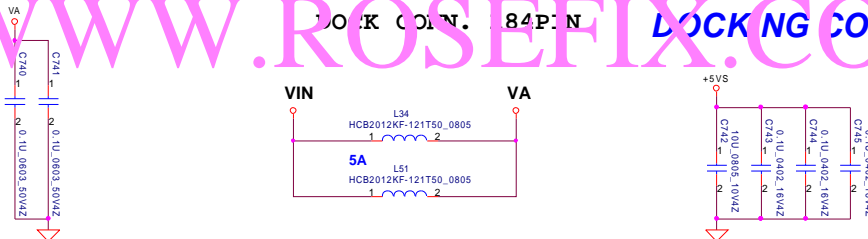
# WLAN/WWAN/BT LED



# TPM1.2 on board

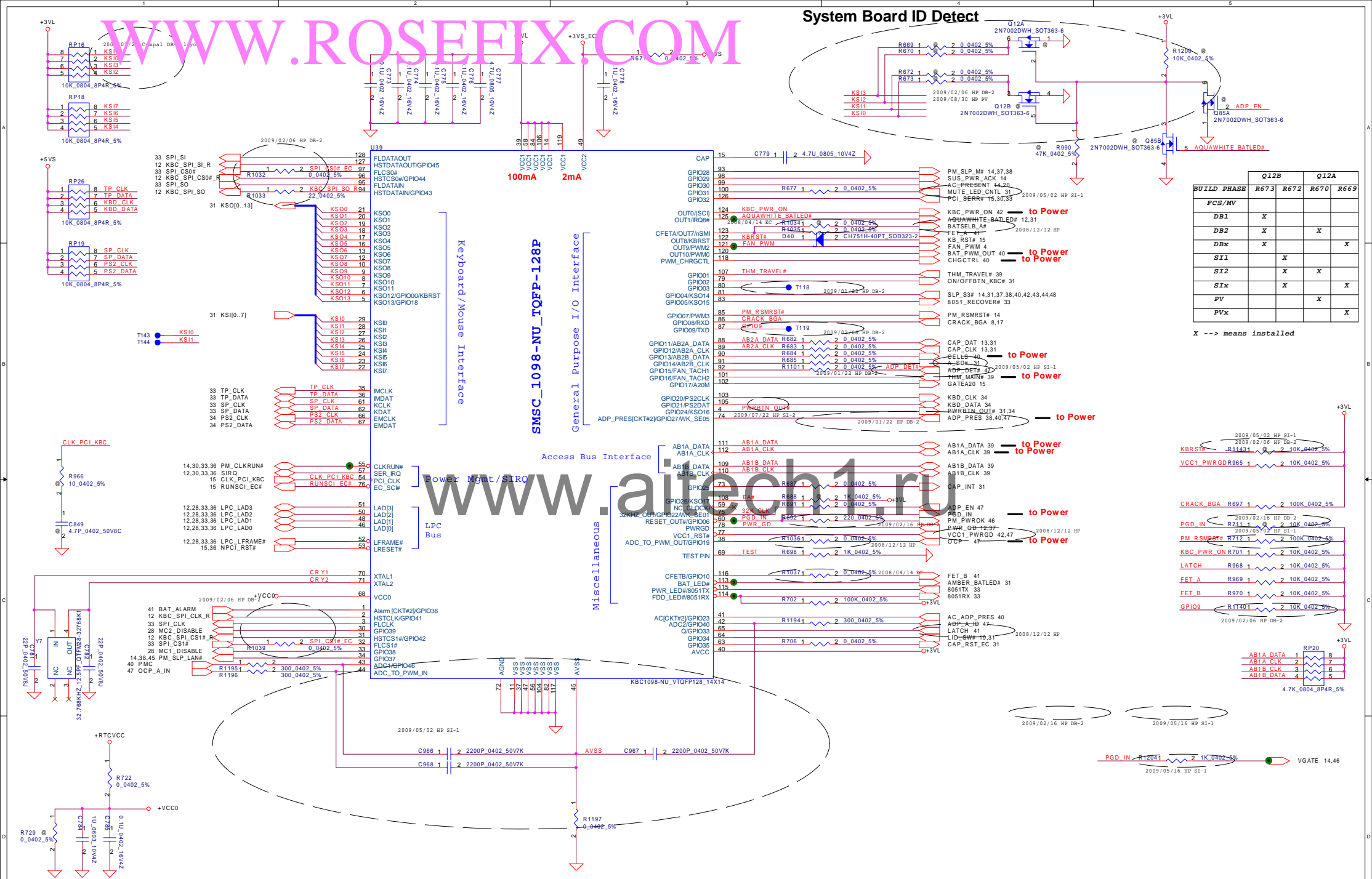


Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2009/12/31	FPR/BIOS/LPC DEBUG/LED/TPM/TP	
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				LA-4901P	Rev 1.0
				Date	Tuesday, December 15, 2009
				Sheet	33 of 54



IN	NC<-->COM	NO<-->COM
L	ON	OFF
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				Custom	LA-4901P	1.0
				Date:	Tuesday, December 15, 2009	Sheet

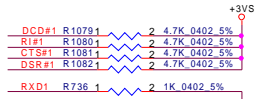
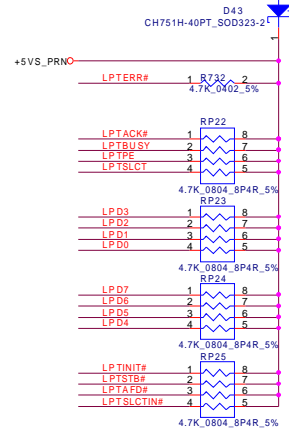


	Q12B		Q12A	
BUILD PHASE	R673	R672	R670	R668
FCS/MV				
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
PVx				X

X --> means installed

## Parallel Port

TO LPC47N217N



34 RXD1

34 TXD1

34 DSR#1

34 RTS#1

34 CTS#1

34 DTR#1

34 RI#1

34 DCD#1

34 LPTINIT#

34 LPTSLOTIN#

34 LPD0

34 LPD1

34 LPD2

34 LPD3

34 LPD4

34 LPD5

34 LPD6

34 LPD7

34 LPTSLOT

34 LPTPE

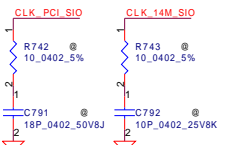
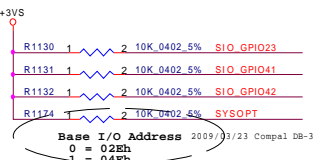
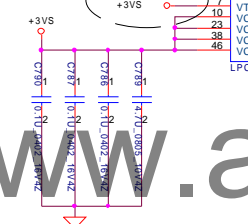
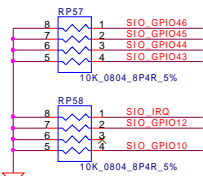
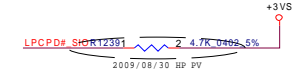
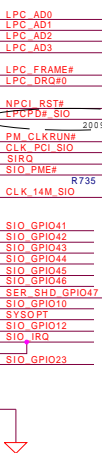
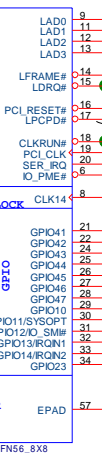
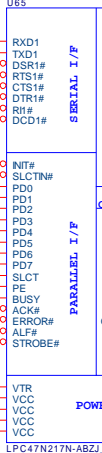
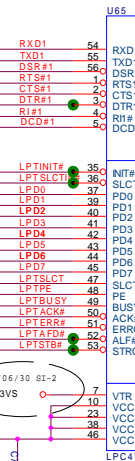
34 LPTBUSY

34 LPTACK#

34 LPTERR#

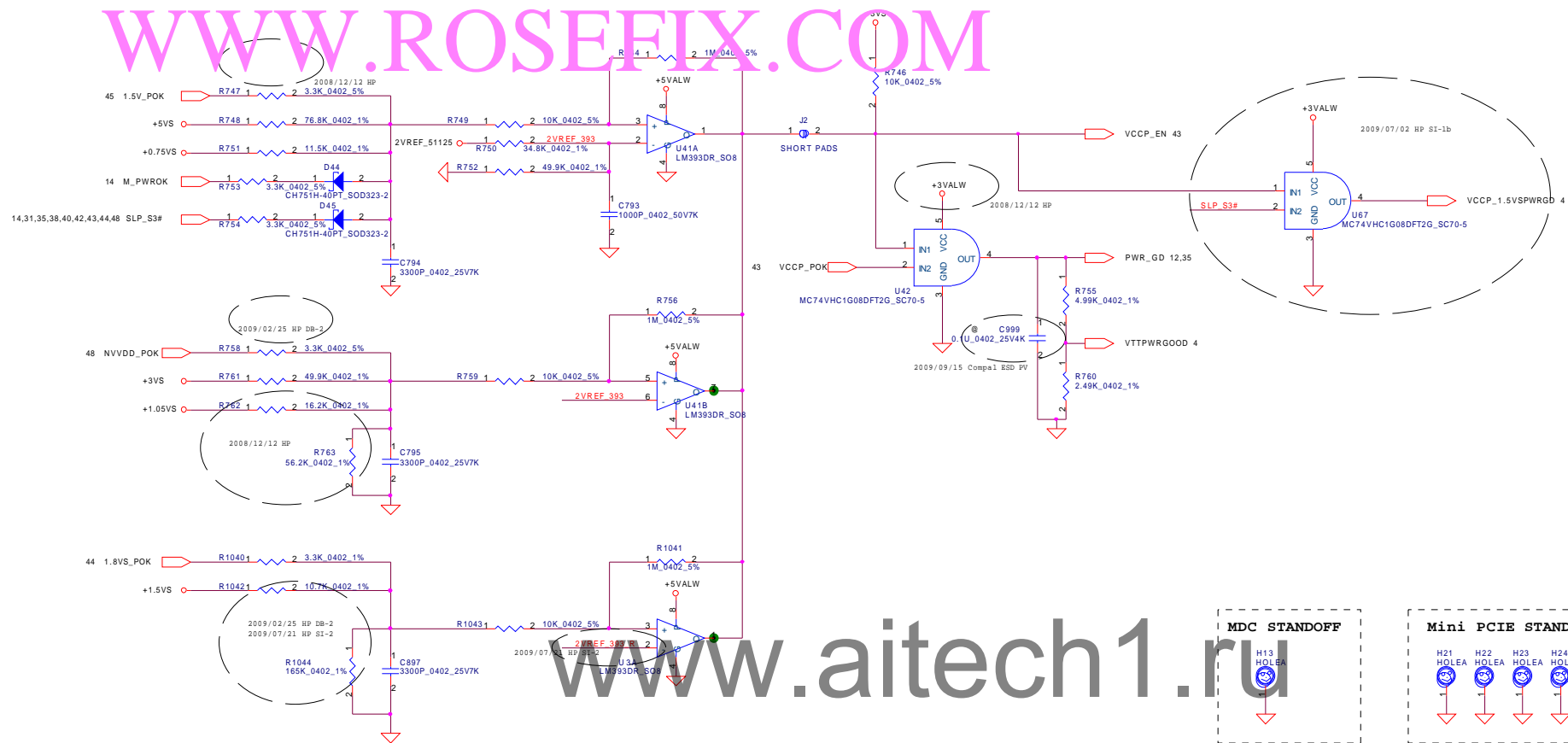
34 LPTAFD#

34 LPTSLOT#

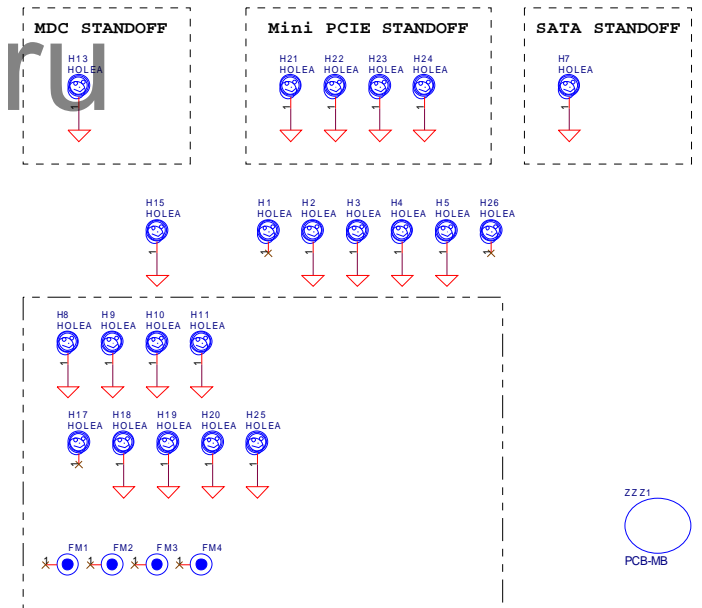


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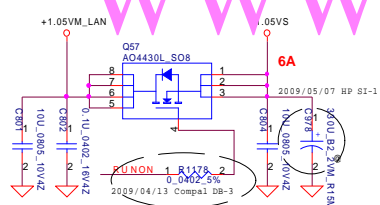
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Issued Date	2008/09/09	Deciphered Date	2009/09/09	Title	SUPER I/O LPC47N217N-ABZJ
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Size	Document Number	LA-4901P		Date	Tuesday, December 15, 2009
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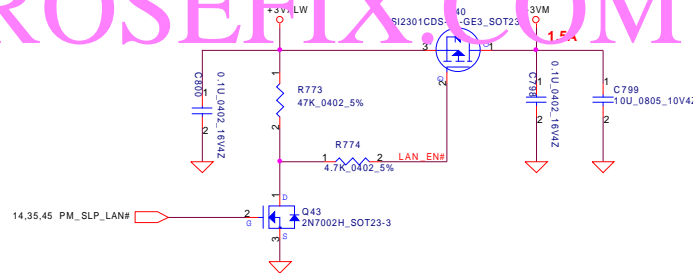
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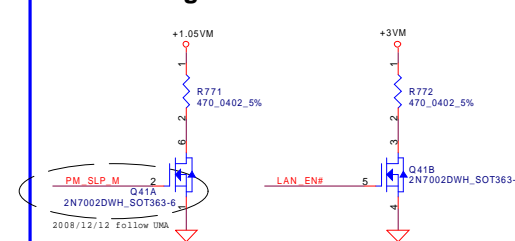
**+1.05V<sub>M</sub> to +1.05V<sub>S</sub> Transfer:**



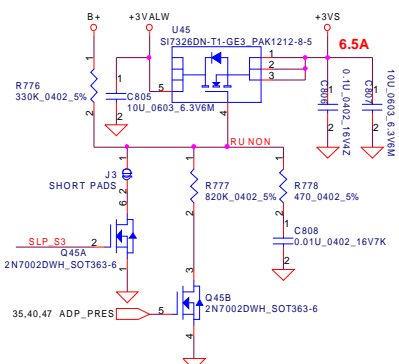
## +3V ALV to +3V M Transfer



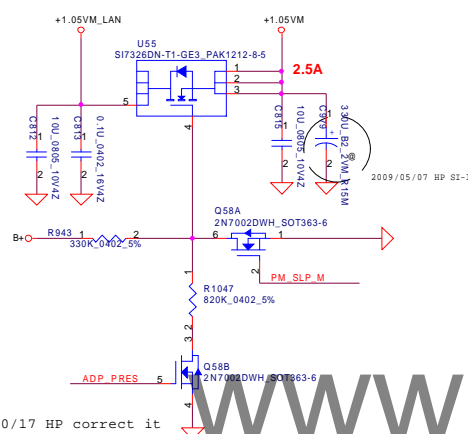
### Discharge circuit-2 for V-M



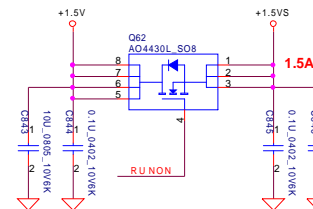
### +3VALW to +3VS Transfer



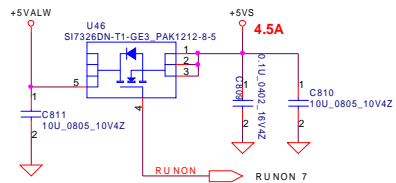
### +1.05VM\_LAN to +1.05VM Transfer



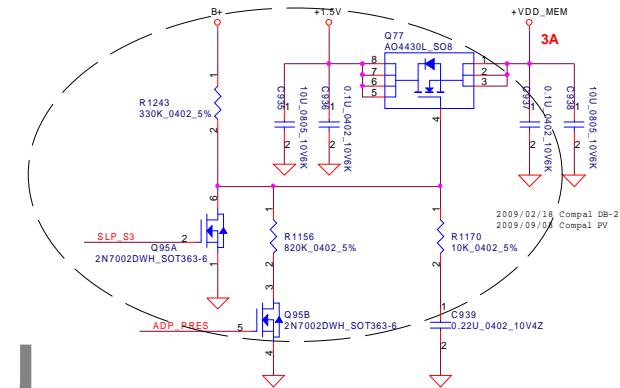
### +1.5V to +1.5VS Transfer



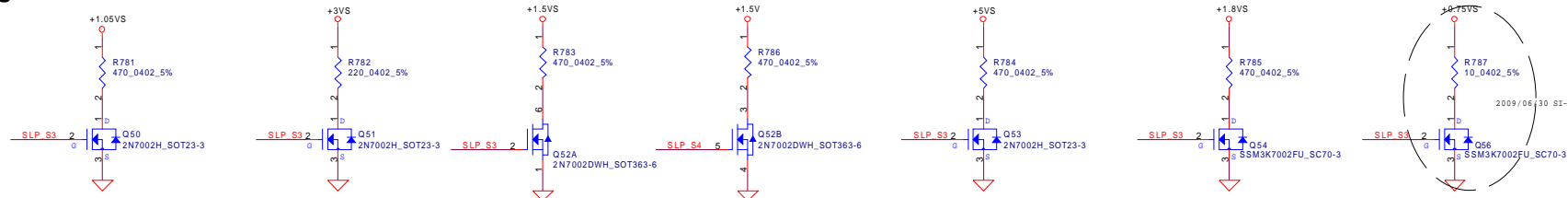
### +5VALW to +5VS Transfer



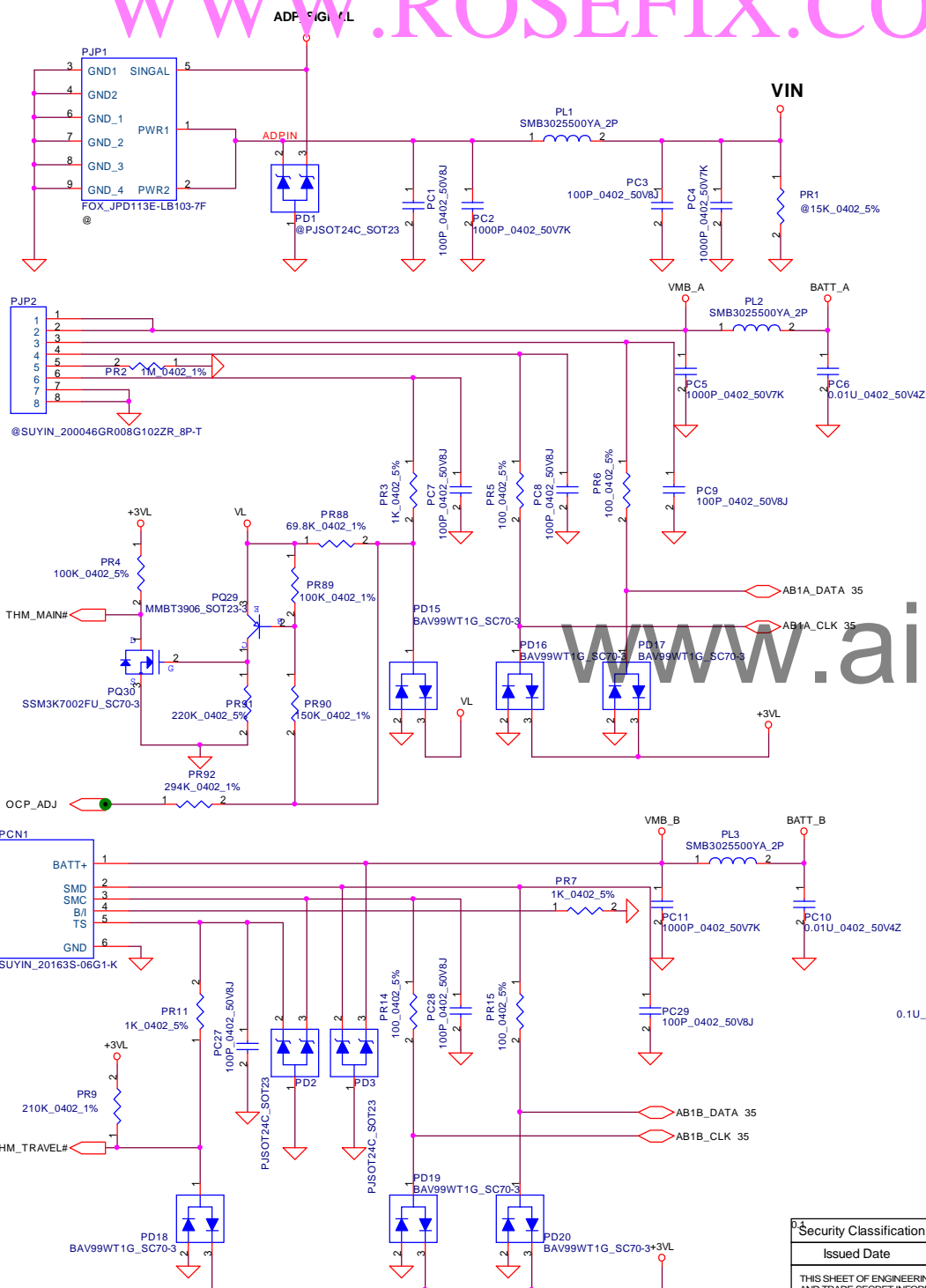
### +1.5V to +VDD\_MEM Transfer



### Discharge circuit-1



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				Size	Document Number <b>LA-4901P</b>	Rev 1.0
				Date:	Tuesday, December 15, 2009	Sheet 38 of 54

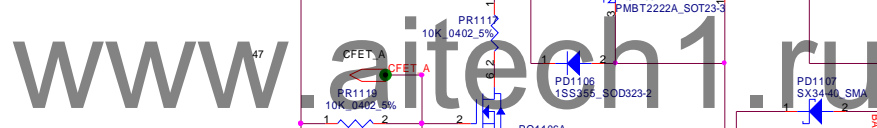


PH1 under CPU bottom side :  
CPU thermal protection at 90 +3 degree C  
(Need to be checked)

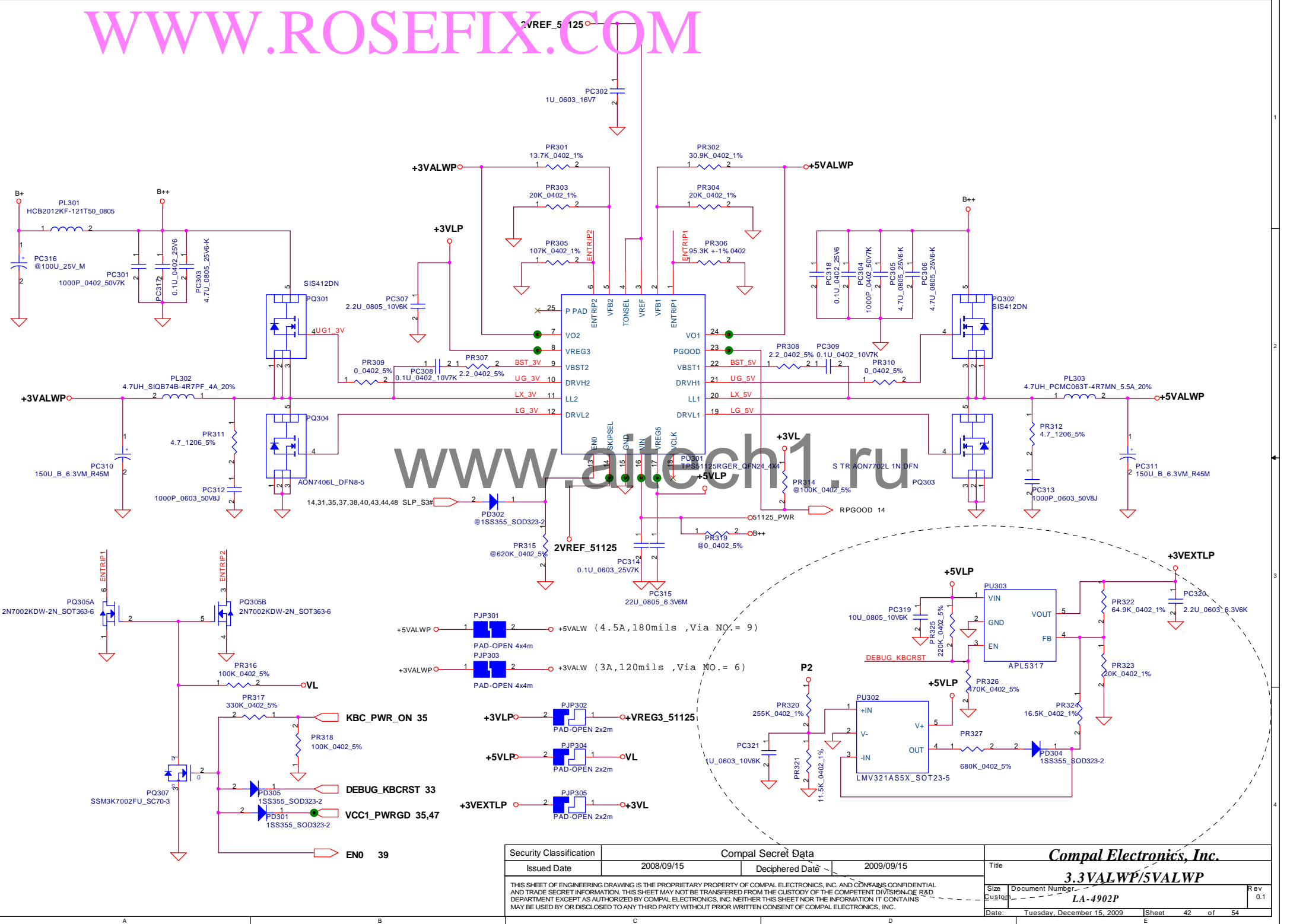
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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	DC-IN/ BATTERY CONN
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				Custom	LA-4902P
				Date:	Tuesday, December 15, 2009
				Sheet	39 of 54



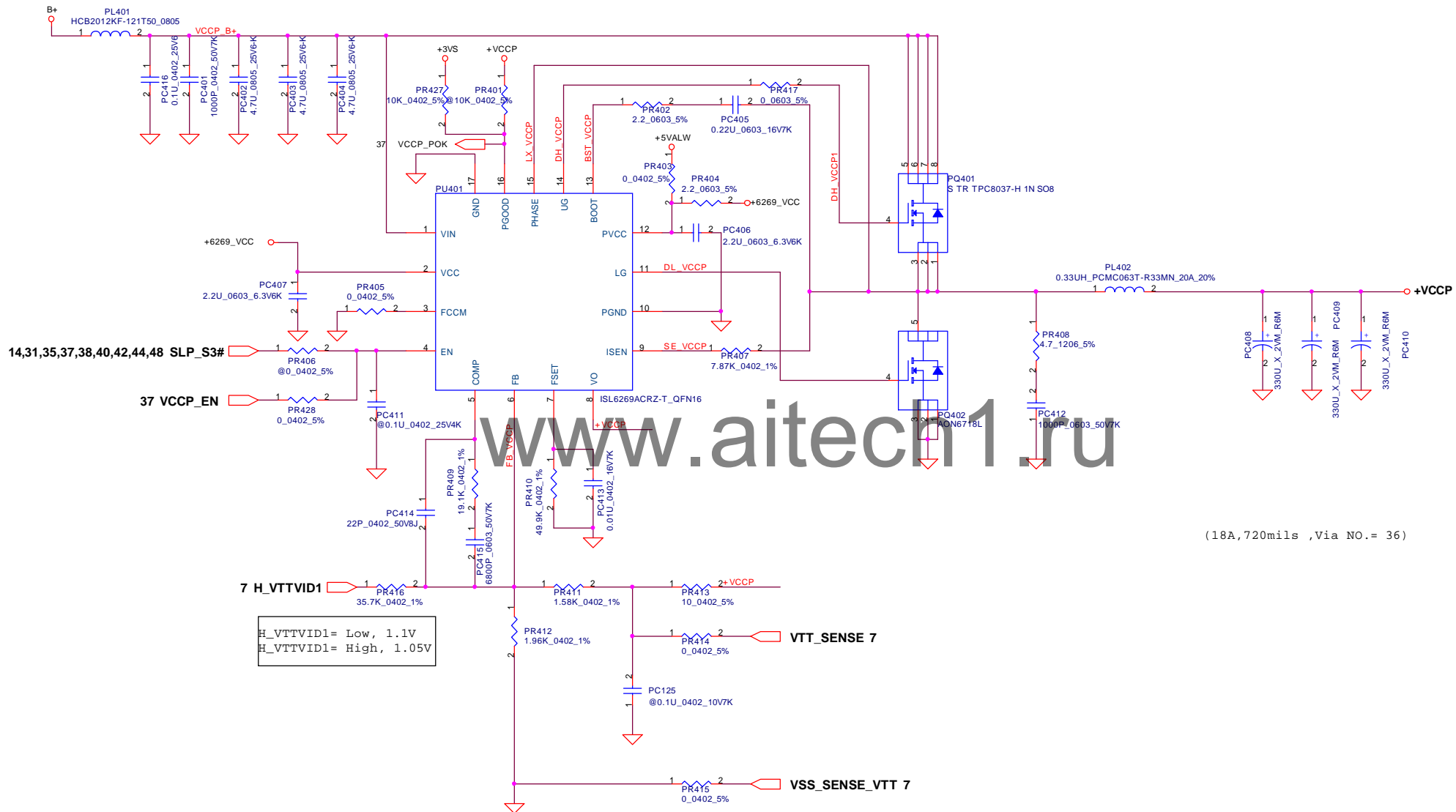
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>				
Issued Date	2008/09/15	Deciphered Date	2009/09/15	<b>Charger</b>				
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				Size	Document Number			Rev
					LA-4902P			0.1
				Date:	Tuesday, December 15, 2009	Sheet	40 of 54	



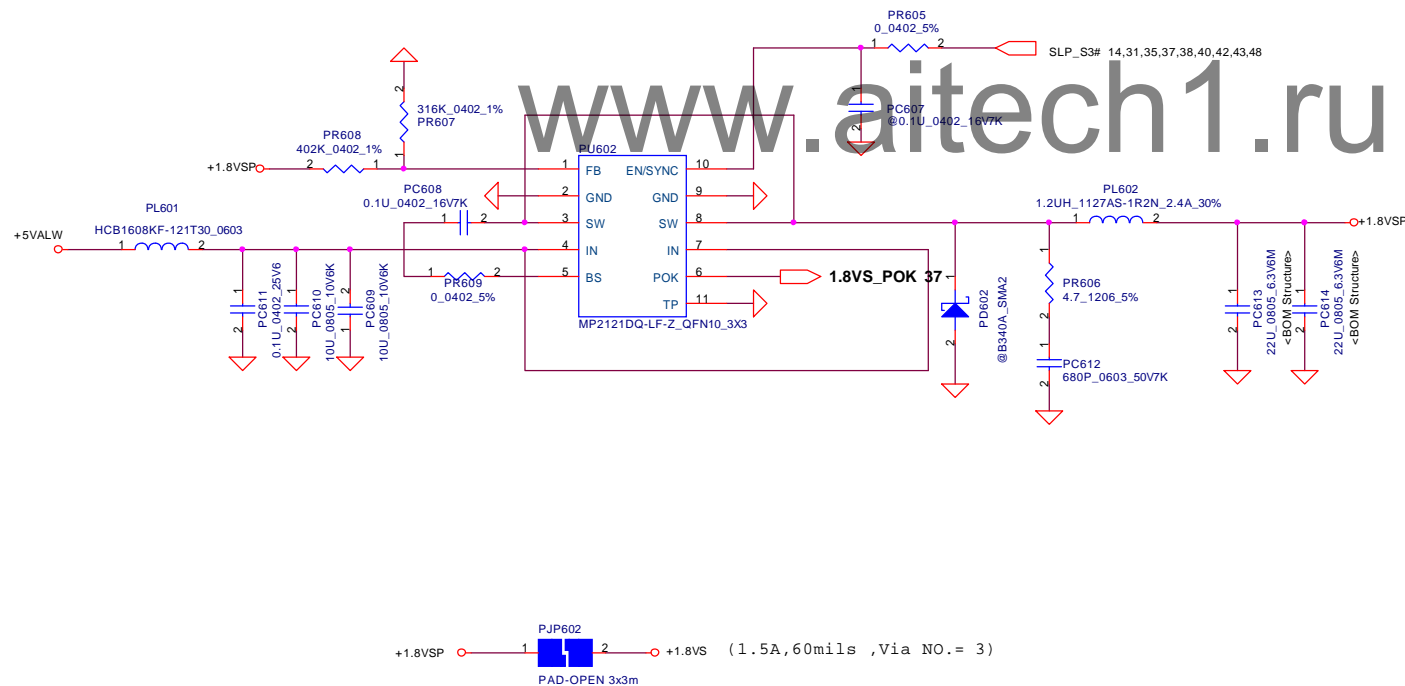
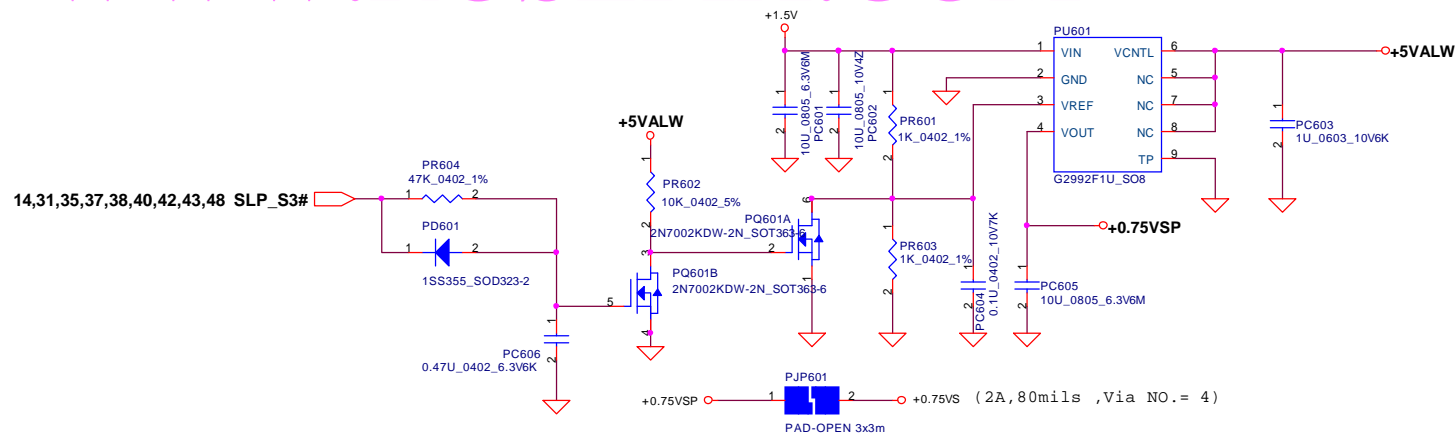
<b>Compal Electronics, Inc.</b>			
Title			
<b>Battery selector</b>			
Size Custom	Document Number <b>LA-4902P</b>		Rev
Date:	Tuesday, December 15, 2009	Sheet	41 of 54



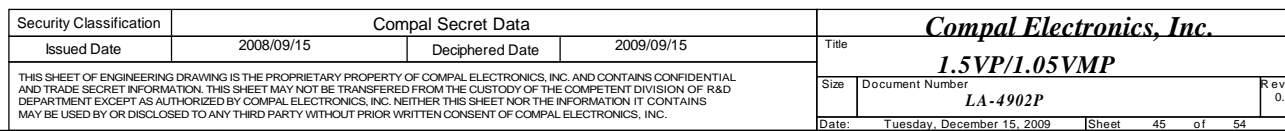
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Size	Custom	Document Number	LA-4902P	Rev 0.1	
Date:	Tuesday, December 15, 2009	Sheet	42	of 54	

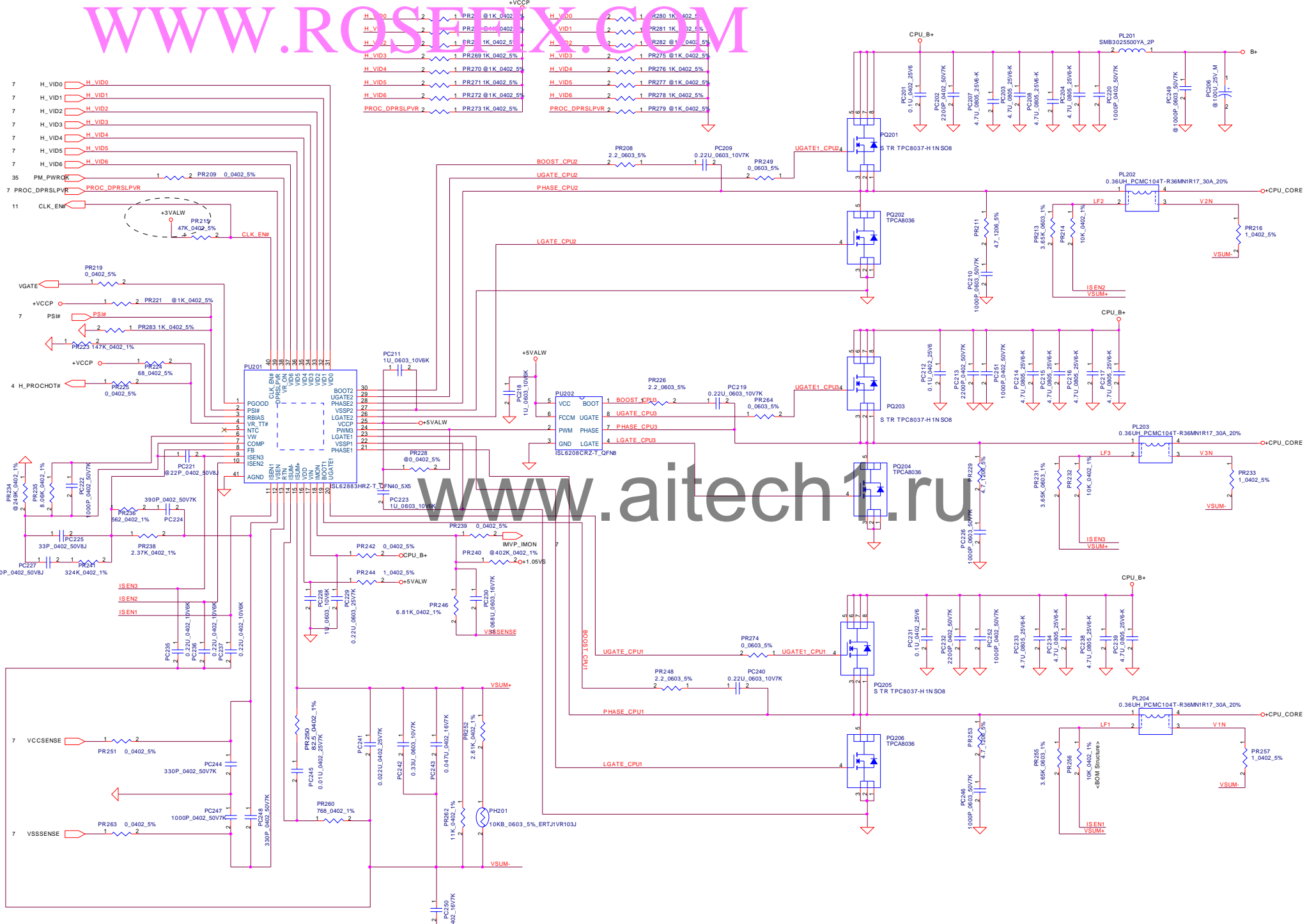


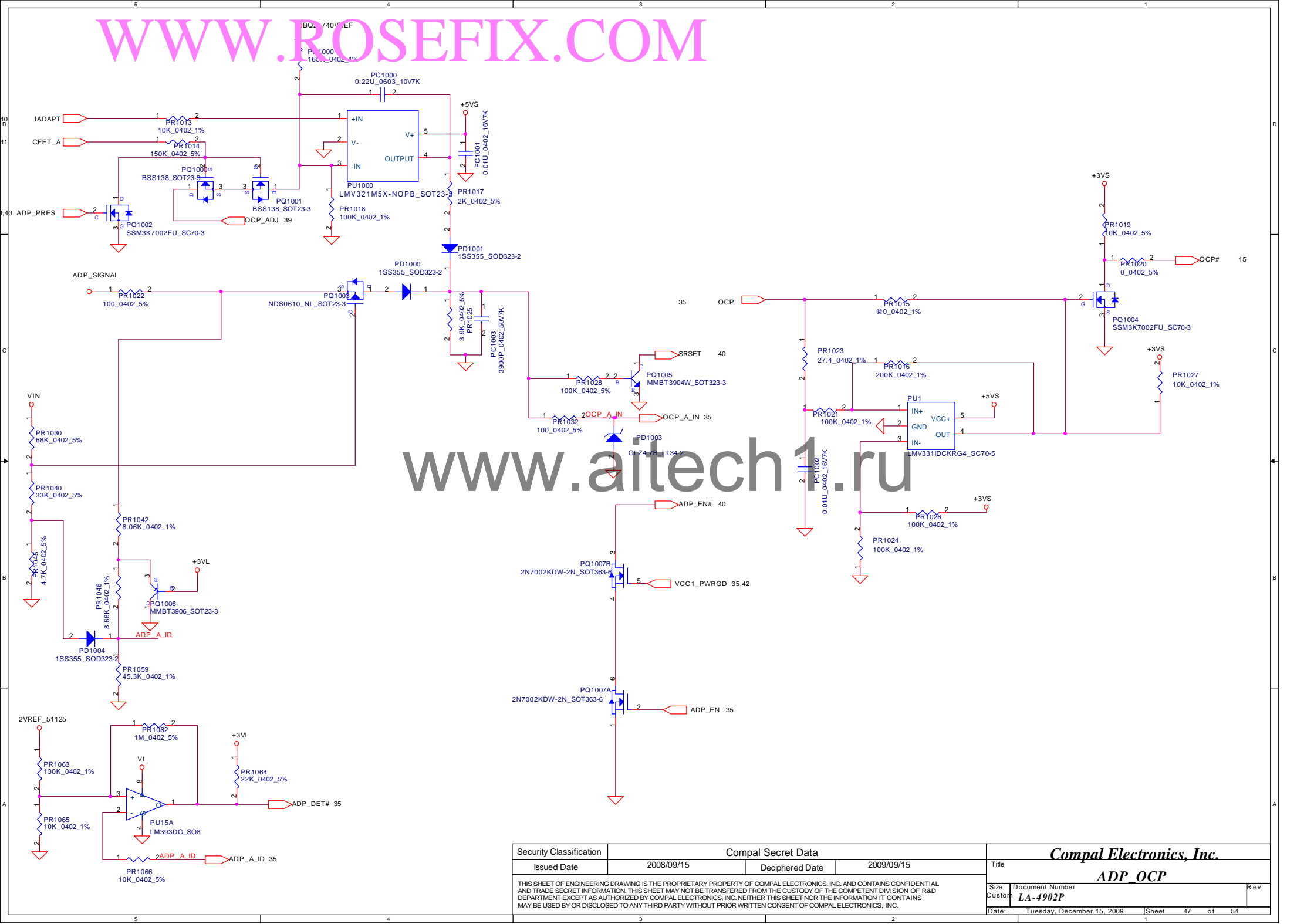
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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	
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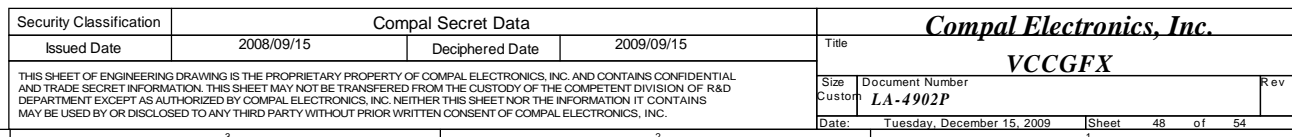






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Size	Custom	Document Number	LA-4902P	Rev	
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## Version Change List (P. 1 of 2) for J W Circuit DB-1 &gt; DB-2

Item	Page #	Date	Request Owner	Solution Description	Rev.
1	01	2009/02/06	HP	Del R4, R6, R8 for XDP.	0.2
2	01	2009/02/06	HP	Del R40 for Thermal sensor.	0.2
3	01	2009/02/06	HP	Del R34, R36, R46, R49, R37 for XDP.	0.2
4	01	2009/02/24	HP	Change R31 24.9K ohm to 1.5K ohm and R33 12.4K ohm to 750 ohm for intel WOW.	0.2
5	01	2009/02/25	HP	Debug port design guide changed XDP debug ports to CFG4 - pin 28, CFG5 - pin 30, CFG10 - pin 22, and CFG11 pin 24.	0.2
6	02	2009/02/19	HP	No install R60, R61.	0.2
7	12	2009/02/25	Compal	Install C193, C194 for WLAN nosie	0.2
8	12	2009/02/06	HP	Change R1026, R181, R185, R1027 from 15 ohm to 0 ohm.	0.2
9	12	2009/02/06	HP	Del C205, C207, C208, C209 for docking.	0.2
10	12	2009/02/06	HP	Change D1 pin 2 form +3VL to +VREG3_51125	0.2
11	12	2009/02/06	HP	Del JP15 pin 51, 53 trace (SMB_DATA_S3, SMB_CLK_S3) and add test point.	0.2
12	12	2009/02/11	HP	Add R1144 1K ohm	0.2
13	12	2009/02/11	HP	Add Test point for SATA bus.	0.2
14	12	2009/02/18	HP	Add NAND Flash dect pin (BRAID_DET)	0.2
15	13	2009/02/06	HP	Install R354	0.2
16	13	2009/02/06	HP	Add R1138 10K ohm	0.2
17	13	2009/02/20	HP	Change R1092, R1093 power sourece form +3VS to +3VS.	0.2
18	13	2009/02/20	HP	Del R208, R210	0.2
19	13	2009/02/22	HP	Add Q76A and Q76B for CBB	0.2
20	13	2009/02/22	HP	Reserve R1146 and R1147 for external VGA thermal	0.2
21	14	2009/01/22	HP	Del R238, because double pull down.	0.2
22	14	2009/02/19	HP	Del R288	0.2
23	14	2009/02/06	HP	Stuff R296	0.2
24	14	2009/02/06	HP	Add R1142 10K ohm	0.2
25	14	2009/02/25	Compal	Add C949 for RF	0.2
26	16	2009/01/22	HP	Del L1, C228, C229 and add test point.	0.2
27	16	2009/01/22	HP	Del L2, C241 and add test point.	0.2
28	16	2009/01/22	HP	Del C847 and add test point.	0.2
29	16	2009/01/22	HP	Del L4, C269 and add test point.	0.2
30	16	2009/01/22	HP	Del L3, C263, C262 and add test point.	0.2
31	16	2009/02/03	HP	Change R299, R300 form 10 ohm to 100ohm.	0.2
32	16	2009/02/03	HP	Change C278 form 0.1uF to 1uF.	0.2
33	16	2009/02/05	HP	Change C243, C244 form 10uF to 22uF.	0.2
34	18	2009/02/18	Compal	Add L48, L49, L50, C944, C943, C942 for EMI	0.2
35	18	2009/02/24	Nvidia	Change R321, R320, R319, R318 form 2.2K ohm to 4.7K ohm.	0.2
36	18	2009/02/18	Compal	Reserve D5, D6, D7, D8, D9 for ESD	0.2
37	18	2009/02/12	Nvidia	Del R1066	0.2
38	19	2009/01/22	HP	Add Q71, Q72, R1134 for Keyboard light	0.2

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## Version Change List (P. 1 of 2, List) for J.W. Circuit DB-1 &gt; DB-2

Item	Page #	Date	Request Owner	Solution Description	Rev.
39	19	2009/02/06	Nvidia	Add C914, C915, C916, C917 for eDP.	0.2
40	19	2009/02/06	HP	Change R341 pin 1 power plan form +5VS to +3VALW.	0.2
41	20	2009/02/12	Nvidia	Reserve R1150	0.2
42	20	2009/02/24	HP	Change R355, R356 from 2K ohm to 10K ohm.	0.2
43	20	2009/02/25	HP	Add Q78, R1158, R1157 for thermal trip.	0.2
44	21	2009/01/20	HP	Del LVDS function	0.2
45	21	2009/02/26	Nvidia	Del C346, because no SPDIF.	0.2
46	22	2009/01/20	Nvidia	Add C924 ~ C931 for DP function	0.2
47	22	2009/02/06	Nvidia	Del RP28, 31, 34, 40, 49, 52, 55, 29, 43, 35, 39, 44, 48, 53, 56, 30, 33, 36, 38, 45, 46, 42 for VRAM	0.2
48	22	2009/02/06	Nvidia	Del C904, 899, 900, 901, 902, 903 for VRAM	0.2
49	23	2009/02/23	Nvidia	Add L47, C941 for SP_PLLVDD	0.2
50	26	2009/02/19	HP	Del C505, C509, C507, C508, C905, Q18, R440, R1062, R441	0.2
51	26	2009/02/06	HP	Add C934	0.2
52	27	2009/02/18	HP	Reserve D57 for ESD	0.2
53	28	2009/02/06	HP	Recover Q25, R503, R483	0.2
54	29	2009/02/26	HP	Add R1159 for NAND Flash detect	0.2
55	30	2009/02/24	Compal	Del R529, R528, R535, C618, U22	0.2
56	30	2009/02/24	Compal	Add Q79 ~ Q83, R1163, R1162, R1164, C945, C946, C947, C948	0.2
57	31	2009/02/22	Compal	Del D30, U28, C711, R608	0.2
58	32	2009/02/18	HP	Reserve D33, D34, D36, D68 for ESD	0.2
59	33	2009/02/18	Compal	Reserve D32 for ESD	0.2
60	34	2009/02/06	HP	Add JP32 of pin 179, 178, 11, 10 to +5VS	0.2
61	34	2009/01/22	HP	Del C746 ~ C761	0.2
62	34	2009/02/06	HP	Add Q75, R1145.	0.2
63	34	2009/02/06	HP	Del R647~ R650	0.2
64	35	2009/02/06	HP	Reserve R711	0.2
65	35	2009/02/06	HP	Add R1140	0.2
66	35	2009/02/16	HP	Change R692 from 10K ohm to 220 ohm	0.2
67	35	2009/01/22	HP	Del L4, C269 and add test point.	0.2
68	36	2009/02/18	Compal	change Super IQ from ITE to SMSC	0.2
69	37	2009/02/25	HP	Del R758	0.2
70	37	2009/02/06	HP	Change R941 pin from PM_SLP_LAN# to PM_SLP_M#	0.2
71	37	2009/02/25	HP	change R1044 from 49.9K ohm to 78.7K ohm.	0.2
72	38	2009/02/18	Compal	Add Q77, R1170, C939, R1156, C935 ~ C938	0.2
73					0.2
74					0.2
75					0.2
76					0.2

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	Hardware revision (0.1 to 0.2)
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Item	Page #	Date	Request Owner	Solution Description	Rev.
01	15	2009/03/23	Compal	Add RP59	0.3
02	15	2009/03/23	Compal	Reserve C956 ~ C951 for RF	0.3
03	30	2009/03/08	Compal	Add R1173 for RF	0.3
04	36	2009/03/23	Compal	Add R1174 10K ohm	0.3
05	36	2009/03/23	Nvidia	Change R1059 from 40.2 ohm to 60.4 ohm	0.3
06	36	2009/03/23	Nvidia	Change R418 from 60.4 ohm to 40.2 ohm	0.3
07	36	2009/04/09	Compal	Install R706 for SMSC CBB	0.3
08	23	2009/04/09	Nvidia	Del L16, C429 ~ C432 for no use LVDS function	0.3
09	23	2009/04/09	Nvidia	Del L17, C433 ~ C435, C436, C437, C883 for no use LVDS function	0.3
10	23	2009/04/09	Nvidia	Add R1175 ~ R1177 for no use LVDS function	0.3
11	18	2009/04/09	HP	Add C957 for DP issue	0.3
12	01	2009/04/13	Compal	Del R12 for follow UMA	0.3
13	38	2009/04/13	Compal	Del Q70, R1094 for follow UMA	0.3
14	35	2009/04/13	Compal	Reserve R1140	0.3
15	31	2009/04/13	Compal	Add R1179 for follow UMA	0.3
16	16	2009/04/13	Compal	Del R290, R291 for follow UMA	0.3
17	15	2009/04/13	Compal	Change C956 ~ C951 from 47P to 22P for RF	0.3
18	04	2009/04/10	HP	Install R51	0.3
19	27	2009/04/10	HP	No install R1083	0.3
20	33	2009/04/10	HP	Reserve R1180	0.3
21	15	2009/04/10	HP	LAN_DIS# should pull up to +3VM_LAN instead of 3VALW	0.3
22	04	2009/04/10	HP	Change R14/R15 to 1.1K1%/3K1% per DGL52	0.3
23	20	2009/04/10	HP	Install R1085 and R1086 for SM communication to GPU	0.3
24	15	2009/04/10	HP	Reserve R1181	0.3
25	19	2009/04/10	HP	Reserve R331	0.3
26	19	2009/04/10	HP	Del R484	0.3
27	09	2009/04/10	HP	Del M2	0.3
28	10	2009/04/10	HP	Del M2	0.3
29	38	2009/04/13	Compal	Add R1178	0.3
30	13	2009/04/10	HP	XTAL_IN (ohm to GND if not used)For discrete:NO INSTALL: R215, Y4, C226, INSTALL 0ohm resistor in C227	0.3
31	35	2009/04/14	Compal	Install R1035, R1036, R1037; no install R1034.	0.3

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Item	Page #	Date	Request Owner	Solution Description	Rev.
01	16	2009/04/24	HP	Del R294	0.4
02	13	2009/04/24	HP	Del CLRP2	0.4
03	14	2009/04/24	HP	Del C147, C148 location	0.4
04	14	2009/04/24	HP	Add C961	0.4
05	14	2009/04/24	HP	Add R1188, R1187 for intel spec	0.4
06	27	2009/04/24	HP	Add C962 ~ C965	0.4
07	36	2009/04/24	HP	Add R1190, R1189	0.4
08	29	2009/04/24	HP	Del C574~C577 and C579~C582.	0.4
09	33	2009/04/24	HP	Add R1191, R1192	0.4
10	26	2009/05/02	HP	Add R1198, R1199	0.4
11	04	2009/05/02	HP	Install R1060	0.4
12	35	2009/05/02	HP	Add R1197, C967, C966, C968, R1195, R1196	0.4
13	38	2009/05/02	HP	Add C978, C979	0.4

Version Change List ( P. I. R. List ) for HW Circuit SI-1>> SI-16

Item	Page #	Date	Request Owner	Solution Description	Rev.
01	04	2009/07/21	HP	Add C997, R1219, Q87, R1218 for CPU S3 power savings issue	0.5
02	04	2009/07/02	HP	Add R1226 for CPU S3 power savings issue	0.5
03	05	2009/07/21	HP	Add Q88, Q89 and reserve R1220, R1222 for CPU S3 power savings issue	0.5
04	07	2009/07/02	HP	Add Q91, R1224, C994, C995, C991, C992, C993, C996, Q92, R1223 for CPU S3 power savings issue	0.5
05	19	2009/06/30	HP	Add R1213, D72 for Lid SW issue	0.5
06	37	2009/07/09	HP	Change C864 from 0.047uF to 0.068uF.	0.5

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Item	Page #	Date	Request Owner	Solution Description	Rev.
01	07	2009/07/22	HP	Change C72 ~ C75 from 10uF to 20uF	0.6
02	11	2009/06/30	Compal	Reserve R1215 for CLK gen change	0.6
03	15	2009/07/23	Compal	Add C949 ~ C951 for Compal RF team.	0.6
04	12	2009/09/03	Compal	Change JBAT1 Connector.	0.6
05	32	2009/09/03	Compal	Reserve Q	0.6
06					0.6
07					0.6
08					0.6
09					0.6
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